/CprE/SE 492 STATUS REPORT 1

1/21/2024 – 1/30/2024

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**
  This week we all resumed our work on the project. This week our analog team created gate level schematics and ran into a frustrating issue with the analog development tools, we plan address this issues and find solutions in the upcoming week.

- **Past week accomplishments**
  - **Noah:** Created gate level schematic of the 90-93 divider and confirmed it operates at lower frequency. I tried to debug REMOVE_ME_PREFIX issue with analog design tools.
  - **Nolan**: Got back up to speed on the Caravel platform so I can start making additions to our project's Verilog code base. Created a blank baseline Caravel project (as a GitLab Tag) that can be branched from to prototype or implement a feature independent from what we have in main. This project does not implement any logic but can be put through the hardening tool and has can go through RTL simulation. I got the toolchain setup on my PC with a Verilog linting tool, which will aid in Verilog development in the future.
  - **Nathan:** Reworked Git repository so that we can begin to directly commit new code to the repository instead of dealing with submodules that ChipForge uses. Began reading up on Verilog constructs necessary to implement Wishbone Crossbar portion of the design.

- **Will:** Began looking into possible open-source options for AES encryption and decryption as well as the possibility of designing it ourselves.
- **Ibram:** worked on the PFD figuring out XSCHEM "REMOVE_ME_PREFIX/" of ngspice .cm files. This problem is currently not fixed.
- **Ethan:** Looked over AES Encryption design provided by Efabless and determined different advantages or disadvantages if it were to be implemented.
- **All Team Members:**

- **Pending issues**
  - **Nolan**: I currently have no issues with what I am working on.
  - **Nathan**
    - No pending issues.
  - **Ibram**
    - Issues with using the standard cell library components without running to the occuring .cm errors.
  - **Will**
  - **Noah**
    - Can't load code models with chip forge analog toolchain

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Noah	Divider schematic and analog bug	10	60
Will	Research AES options	5	49
Ethan	Research on Efabless AES provided design	3	47
Ibram	XSCHEM fixing issues.	5	52
Nathan	Git repository rework, Verilog research	5	58.5
Nolan	Refamiliarizing with Caravel platform, blank baseline project creation, local toolchain installation.	6	61

- **Plans for the upcoming week**
  - **Will:** Continue to research AES options and begin narrowing down options.
  - **Nathan**
  - **Ibram** start designing another component until there is a fix to the XSCHEM issue.

- **Nolan**: Start developing the Caravel Project Helper tool, which will allow us to easily incorporate multiple Verilog files into our project. It took longer than I thought to get a blank baseline Caravel project since it has been a bit since I have worked with the Caravel platform directly. But since everything is set up, I can create a basic project that contains multiple Verilog files, verify that it is functional, and then write the helper tool. The project that contains multiple Verilog files will be used as a baseline to make sure the tool is functional.
- **Ethan:** Determine specifics on AES design provided by Efabless, look through other open-sourced options.
- **Noah** debug analog toolchain, replace jk flipflops with d flipflops in divider schematic, create schematic for accumulator and control register

- **Summary of weekly advisor meeting**

We discussed the divider schematic, plans for implementation, and standard library usage. Our plans for moving forward with implementation have been discussed with our advisor and approved.