CprE/SE 492 STATUS REPORT 2

2/04/2025 – 2/13/2025

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

  This week we continued to work on different parts of our project. AES open-sourced options were investigated to determine which options suit our project the best. The digital team continued to work on the wishbone bus and the Verilog helper tooling. The analog team developed the PLL design and schematic further.

- **Past week accomplishments**
  - **Noah:** Completed divider gate level design. Specifically, I created the design for the accumulator.
  - **Nolan**: Finished the Verilog Helper tool, which will allow us to easily add and remove Verilog source files from our project. In addition, I worked on getting a RISC-V core instantiated and put into the project.
  - **Nathan:** Continued work on Wishbone crossbar, specifically focusing on making it configurable so we can easily support different numbers of masters and slaves connected to the crossbar.
  - **Will:** Did research on open-source IP AES encryption options, listing pros and cons for each option I found and providing details on the specifications and documentation for each one.
  - **Ibram:** Finished the PFD schematic design and made simulations ensuring that it meets the designed specifications

- **Ethan:** Conducted research on AES encryption options, with a focus on the one provided by Efabless. Found specific details important to the project, such as FMax (20 MHz) and 520x520 µm die space required.
- **All Team Members:**

- **Pending issues**
  - **Noah**: Test analog tool chain fix to confirm it will be fabricated correctly
  - **Nolan**: I have no pending issues currently.
  - **Nathan:** No pending issues at this time.
  - **Will:**
  - **Ibram:** None
  - **Ethan:** None

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Noah	Accumulator design	5	65
Will	Open-source AES encryption research	6	55
Ethan	AES Research and specific documentation / hardware details for each	6	53
Ibram	Ran schematic simulations for the PFD	10	62
Nathan	Further crossbar work.	6	64.5
Nolan	Finished Verilog Helper. Worked on instantiating a RISC-V core.	7	68

- **Plans for the upcoming week**
  - **Will:** Continue research of open-source AES options to figure out which will fit best in implementing the ZigBee standard. Add our analysis and research of AES options to the design document.
  - **Nathan:** Continue work on crossbar and begin running it through tapeout and creating documentation.
  - **Ibram:** I will work on designing the VCO
  - **Nolan**: I will be instantiating a RISC-V core that has a wishbone interface to the instruction and data memory segments. I also plan to instantiate some DFF RAM (D-Flip-Flop RAM) so I can provide the RISC-V core some instructions and some RAM.

- **Ethan:** Continue to add more documentation to design documents, add diagrams, be more specific about AES requirements when it comes to NIST standards and ZigBee standards, to support choices. Harden the different AES choices to provide better reasoning behind choices.
- **Noah:** Implement divider design in analog toolchain and begin testing if possible.

- **Summary of weekly advisor meeting**

We discussed the different AES open-sourced options and discussed the need for design specific details in regard to requirements set by the Zigbee standard the NIST standard that we chose to follow.