CprE/SE 492 STATUS REPORT 4

2/27/2025 – 3/13/2025

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**
  This week each team (digital, analog, and security) continued to work on different parts of the project. Each team member is working on a different part or component of the project on their own before we start adding and integrating parts together. Specifics on the different components that each member worked on is outlined in the past week accomplishments.

- **Past two weeks accomplishments**
  - **Noah:** Debugging full divider design, testing all 26 possible inputs
  - **Nolan**: I continued to work on writing tests for the DFF RAM wishbone slave interface module. The tests I have are currently passing and test most of the signals coming in and out of the DFFRAM module. I also started the process of hardening the design, which is where I ran into issues.
  - **Nathan:** Work was completed on the automatic generation script and tested crossbar. The crossbar complies with Wishbone standards and sends and receives data as expected.
  - **Will:** Continued AES encryption documentation and putting the research into the design document.
  - **Ibram:** Continued with VCO simulation

- **Ethan:** Worked on message authentication codes and CCM* encryption method in AES module. Security subsystem document & AES diagrams.
- **All Team Members:**

- **Pending issues**
  - **Noah**: Accumulator not properly resetting when counting by nine
  - **Nolan**: I am currently running into issues during the place and route portion of the hardening process for my DFF RAM slave interface. I have some people I can reach out to and some more information about the errors, so I should be able to get the design to harden soon.
  - **Nathan:** No current outstanding issues are present, Wishbone crossbar is continuing to be tested and issues will be fixed as they arise.
  - **Will:**
  - **Ibram:** parameter sweep and frequency simulation is taking time. I am reached out to ChipForge and the online open-source community for support.
  - **Ethan:** CCM* mode not authenticating message codes properly

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours last two weeks	HOURS cumulative
Noah	Divider debugging and simulating all inputs	10	101
Will	AES research & documentation, updating design doc	10	70
Ethan	MAC and CCM*, Security Subsystem document	12	71
Ibram	Continued with VCO simulations	10	92
Nathan	Crossbar script and testing	10	86.5
Nolan	Wrote more DFF RAM slave interface tests. Made good progress hardening the design.	10	78

- **Plans for the upcoming week**
  - **Will:** Finish updating the design document with AES information and work towards integrating encryption with the rest of the software
  - **Nathan:** Continue crossbar testing and integrate into main design.
  - **Ibram:** Finish VCO simulation and start designing the charge pump.
  - **Nolan**: For the next two weeks I plan on getting my DFF RAM slave interface module to harden. Once the module has been hardened, I can generate a gate-

level netlist, which will enable me to run gate-level tests. Then once the gate-level tests are passing, I will be hooking up the DFF RAM to the generated RISC-V core.

- **Ethan**: Get CCM* encryption working, finish Security Subsystem doc.
- **Noah:** Fix issues divider, start layout

- **Summary of weekly advisor meeting**

  The advisor meeting this week largely consisted of continued discussion on the progress of each team and their development of each component. The security subsystem document was reviewed and needs additions to citations and references to documents relating to the specific standards our project is based on, tables to simplify information, and clarification on why hardware acceleration and encryption is necessary. The digital team presented their progress, which included a functional Wishbone crossbar and simulated DFF RAM. The digital team also encountered issues related to simulating the DFF RAM at the gate level, which is currently being investigated.