CprE/SE 492 STATUS REPORT 4

3/13/2025 - 4/3/2025

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

  This week, the digital team was able to completely finish the crossbar and fix bugs related to the DFF RAM tool flow tests. The team is currently in the process of starting integrating the crossbar, the RISCV core and the RAM modules. The analog team was able to fully finish the schematic, layout, and simulations of the voltage controlled oscillator. They fixed some bugs related to the divider schematic and started layout of the pre-scalar divider subcircuit. The team discussed various layout techniques of the charge pump and the pre-scalar circuits with Dr. Neihart. The security team finalized the security portion of the design document. They are currently working on instantiating the AES encryption module.

- **Past two weeks accomplishments**
  - **Noah:** Finished pre layout testing of the divider. Completed initial prescaler layout and revised it. With feedback from Dr. Niehart
  - **Nolan**: These past two weeks I continued researching the OpenLane tool and configuration files in hopes of getting the project with the DFF RAM macros to fully go through the flow. I made good progress on this but was not able to fully get things to go through the flow. I then switched gears and finalized my DFF RAM tests, integrated two RAM modules, the Vex RISCV core, and merged my changes to our main GitLab repo.

- **Nathan:** Completed Wishbone Crossbar, tested it, and merged it back into the main branch of the repository. Crossbar is generic, so it can easily be expanded as the design grows.
- **Will:** I helped finalize the security portion of the design document.
- **Ibram:** VCO schematic, layout, post-layout simulations complete. I also started the charge pump schematic.
- **Ethan:** Worked on getting the CCM* mode working, still working on the MAC working.
- **All Team Members:**

- **Pending issues**
  - **Noah**: None
  - **Nolan**: I am still having issues getting the project with the RAM macros to fully go through the flow.
  - **Nathan:** None
  - **Will:**
  - **Ibram:**
  - **Ethan**: None

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours last two weeks	HOURS cumulative
Noah	Prelayout testing. Prescaler layout	32	133
Will	Finalized security portion of design document	10	80
Ethan	Worked on CCM* mode for security acceleration and MAC for data security	12	83
Ibram	VCO is completely finished	55	147
Nathan	Finished Wishbone Crossbar.	16	102.5
Nolan	OpenLane research and configuration changes, finalizing DFF RAM tests and merging to main.	16.5	94.5

- **Plans for the upcoming week**
  - **Will:** I plan to work towards integrating the security subsystem in with the rest of the software.
  - **Nathan:**
  - **Ibram:** I plan to finish the charge pump schematic and integrate it with the PFD.

- **Nolan**: I plan on still looking into why the project won't fully go through the OpenLane flow when the DFF RAM macros are instantiated. In addtion, I plan on starting to design an I2C controller for the project.
- **Ethan**: Finish security acceleration with the MAC working, test on FPGAs, work on integration with rest of digital
- **Noah:** Extract layout and simulate. Integrated prelayout simulation of the PLL.

- **Summary of weekly advisor meeting**

  We mainly discussed the team's progress for the past week and discussed next steps of fully integrating the PLL and start testing its parameters. This along with integrating and testing the digital components together. We also discussed the possibility of flashing the integrated digital design on an FPGA. For the security component of the project, we briefly discussed completing the AES encryption module and integrating it with the rest of the digital design.