CprE/SE 492 STATUS REPORT 6

4/3/2025 - 4/17/2025

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

  The past two weeks, our team has been busy with our respective tasks on the digital, analog, and security domains. The digital team has been integrating the generated RISC-V core into the system and looking into developing an I2C controller. In addition, some test updates were made and some investigations on running gate-level tests were conducted. The analog team continued to work on the layouts for the divider and other analog components. In addition, LVS and parasitic extraction have been worked on for the divider, but it is not fully complete yet. Finally, the security team has been working on updating the design document to include new decisions made and any new security-related information.

- **Past two weeks accomplishments**
  - **Noah:** Worked on design document updates, including implementation of the divider. Finished layout for the divider. I made progress of LVS and extraction.
  - **Nolan**: These past two weeks I worked on updating my DFF RAM tests to work after the integration with the crossbar. I was able to also make a few optimizations to the hardware description and removed some parts of the test that were put there by assumption. I also started to work on a hardware description for a wishbone compatible register file. The design is almost done and currently needs a test written for it. This will be used in the I2C module I will be working on in the next

few weeks. Finally, I also worked on getting the gate-level version of my DFF RAM test to work, but ran into some issues with the wishbone signals.

- **Nathan:** Worked on design document updates to document implementation for Wishbone crossbar and to update risks and requirements based on events this semester. Merged code from Nolan's branch into integration branch to continue work on getting second RISCV core to run.
- **Will:** Worked on updating the design document to include more information on the security subsystem.
- **Ibram:** I almost completed the charge pump design. I went back and redesigned the VCO to use 3.3V instead of 1.8V and used a different NMOS/PMOS family due to the increased voltage. Documented some of my VCO design.
- **Ethan:** Worked on testing security architecture after finalizing message authentication codes (MAC)
- **All Team Members:**

- **Pending issues**
  - **Noah**:
  - **Nolan**: The DFF RAM gate-level test is not working currently, but I have moved on to working on the wishbone compatible register file and the I2C module, so this will not affect my progress.
  - **Nathan:** None
  - **Will:**
  - **Ibram:**
  - **Ethan**: None

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours last two weeks**	**HOURS cumulative**
Noah	Design document, Layout, LVS, Extraction	16	149
Will	Design document work	7	87
Ethan	Security Encryption Testing	6	89
Ibram	VCO re-design. Charge pump design	10	157
Nathan	Design document work and work on second RISCV core booting.	14	116.5
Nolan	Gate-level test investigation, wishbone compatible register file development, DFF RAM optimization update and test update	14	108.5

- **Plans for the upcoming week**
  - **Will: Continue** working on design document.
  - **Nathan:** Keep working to try and get the second RISCV core to run a program.
  - **Ibram:** finish the charge pump and test it. Complete the layout of the high voltage VCO design.
  - **Nolan**: I will continue to work on the wishbone compatible register file and the I2C module and will investigate getting the gate-level tests to work.
  - **Ethan**: Add additional testing to security architecture, work on integrating with other digital components.
  - **Noah:** Extract layout and simulate divider

- **Summary of weekly advisor meeting**

  In our advisor meeting, we presented the progress we made over the week and went over the design document as instructed by the design document review Canvas assignment. We presented any concerns we had with the state of the document as well as asked for advice on how to go about updating some sections. Overall, the meeting was quite informative and gave us some direction on how we should proceed updating some of the sections in the design document.