Open-Sourced Radio Microcontroller for Fabrication

ECPE Senior Design May 2025, Team 27

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Faculty Advisor and Client: Dr. Henry Duwe

Team Website: https://sdmay25-27.sd.ece.iastate.edu/

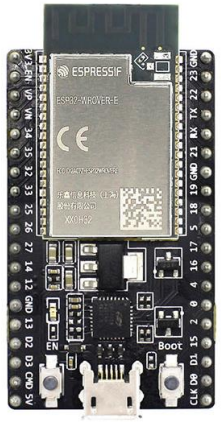
References to Design Document on slides as DD <page number>

IOWA STATE UNIVERSITY

Problem Statement

- Existing **radio** microcontroller units (MCUs) have closed source designs
- Difficult for ISU students, ChipForge (ASIC design ISU club) members, and radio hobbyists to learn about how **radio** MCUs work
- Need an open-source MCU design that can be fabricated (silicon proven)

Closed Source Radio MCUs



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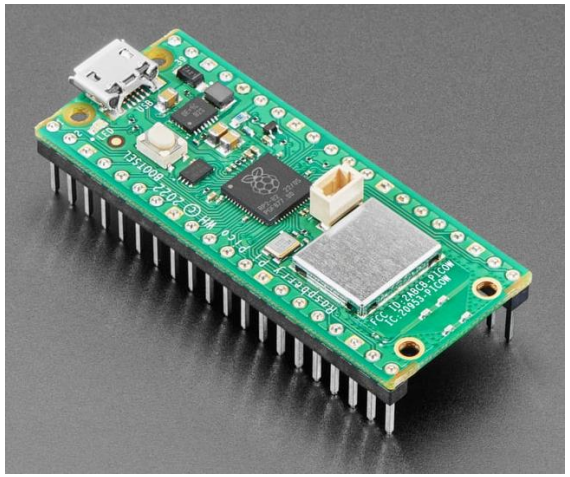

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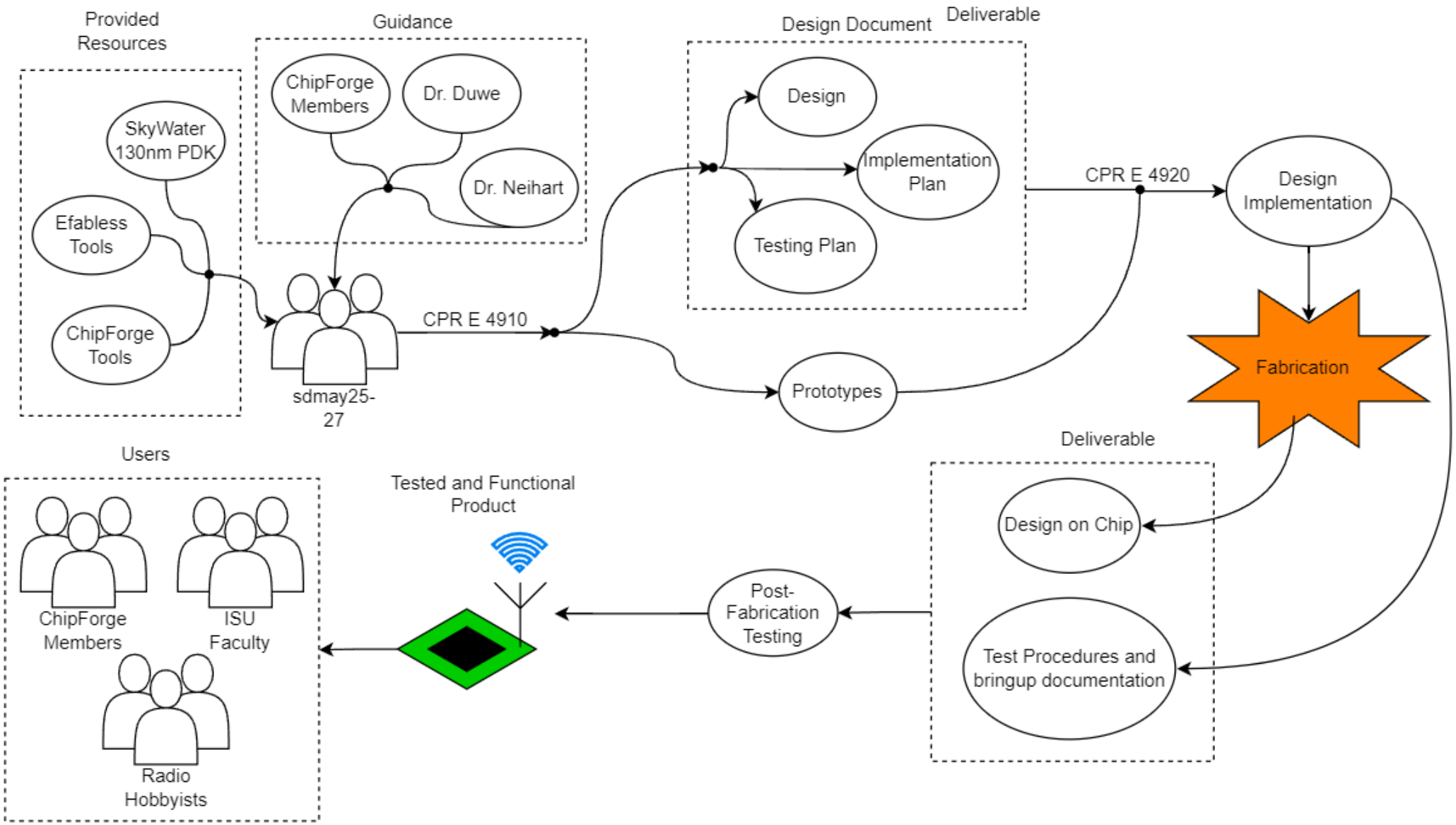
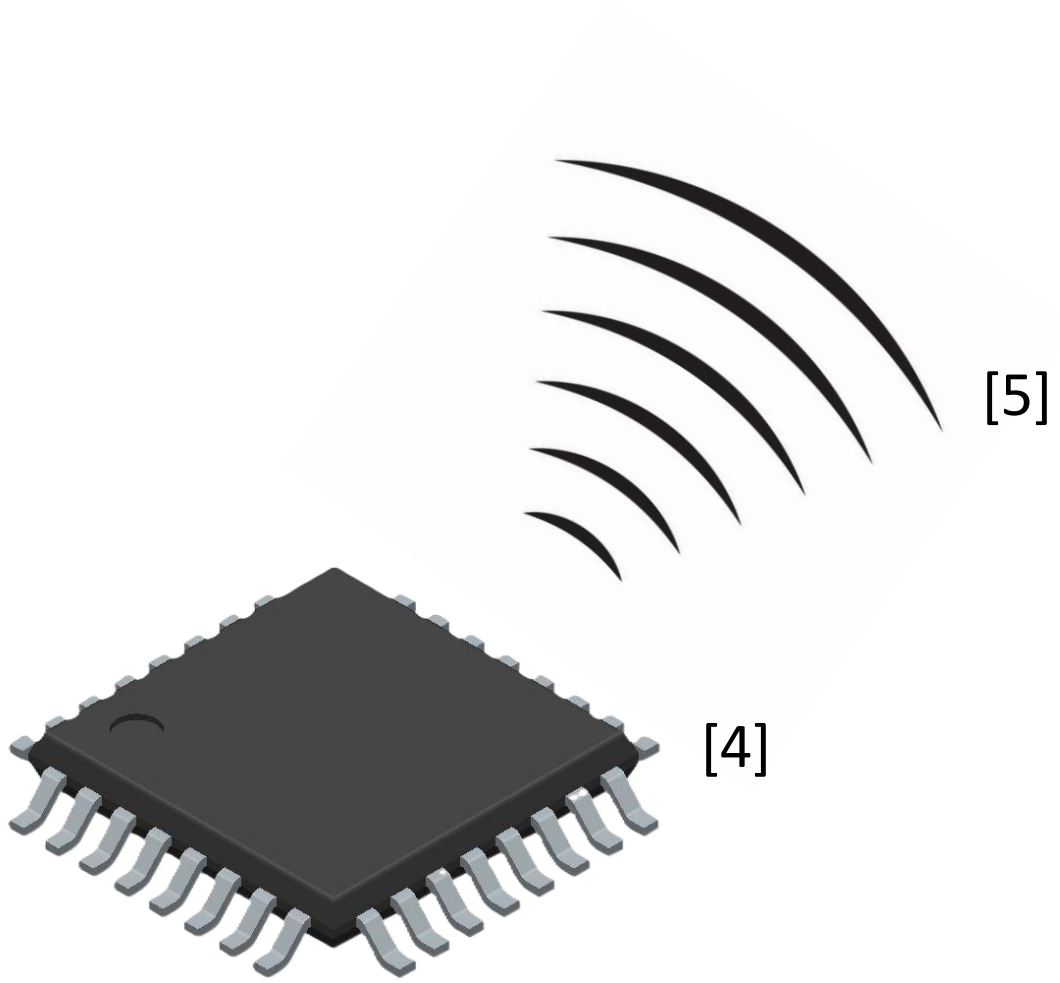
Conceptual Sketch/Solution



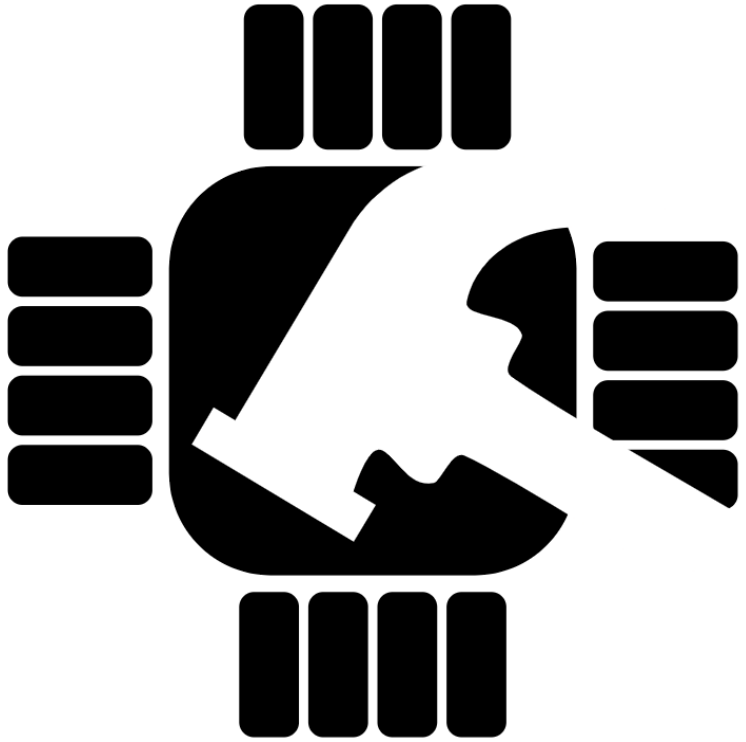
Functional Requirements

- MCU shall implement an open standard wireless protocol stack
- We will provide software libraries providing access to hardware functions
- MCU shall contain a radio subsystem
  - The radio subsystem shall support the Zigbee 915Mhz operating frequency
- The radio signal's phase noise will be below -41dBm/100Hz at a 32MHz offset per IEEE standard 802.15.4
- The radio signal's spurious emissions will be below -20dBc per IEEE standard 802.15.4
- DD 14-15


[5]
[4]

Non-functional Requirements

- All the artifacts produced throughout the design of the MCU shall be open source.
- Thorough documentation usable by students with only basic knowledge of circuits and digital logic.
- Our documentation is targeted toward the ISU co-curricular Chip Forge.
- DD 16-17

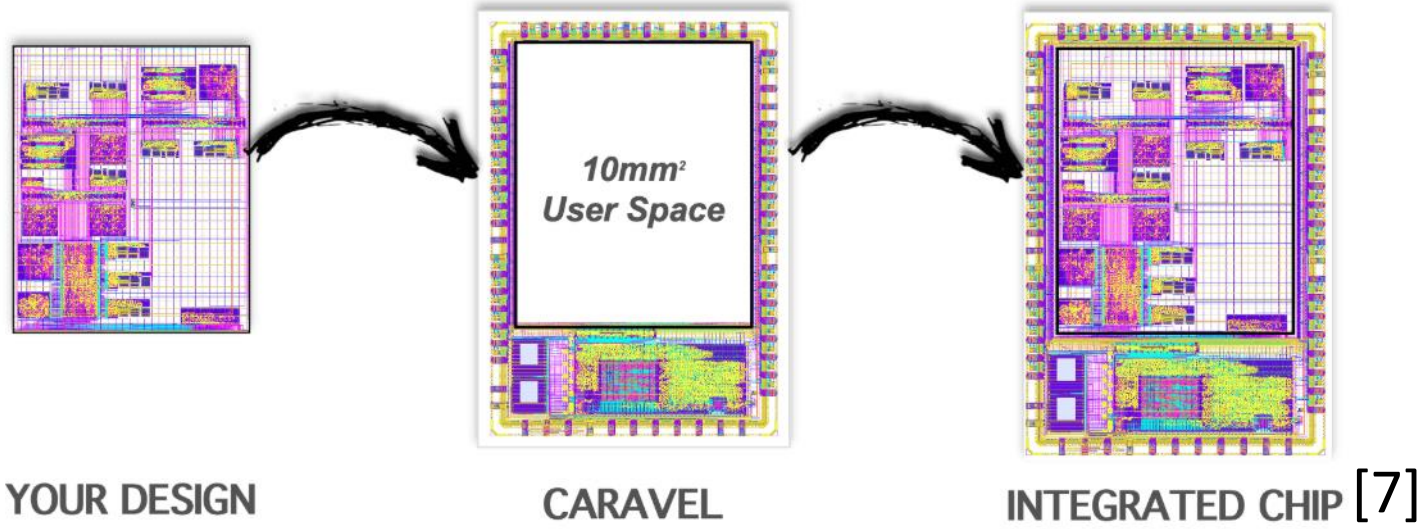


[6]

Technical/Other Constraints

- Must use Efabless process and associated tools
  - Must be fabricated in the SkyWater 130nm process
  - No flexibility on this, given by client
- Die space limited to 2.92 mm x 3.52 mm
- Design must be open-source
  - Unable to use IP from many vendors due to closed-source nature
- DD 16

[8]



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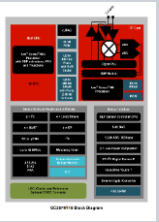
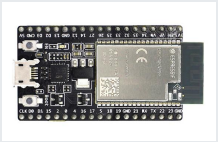
Market Research

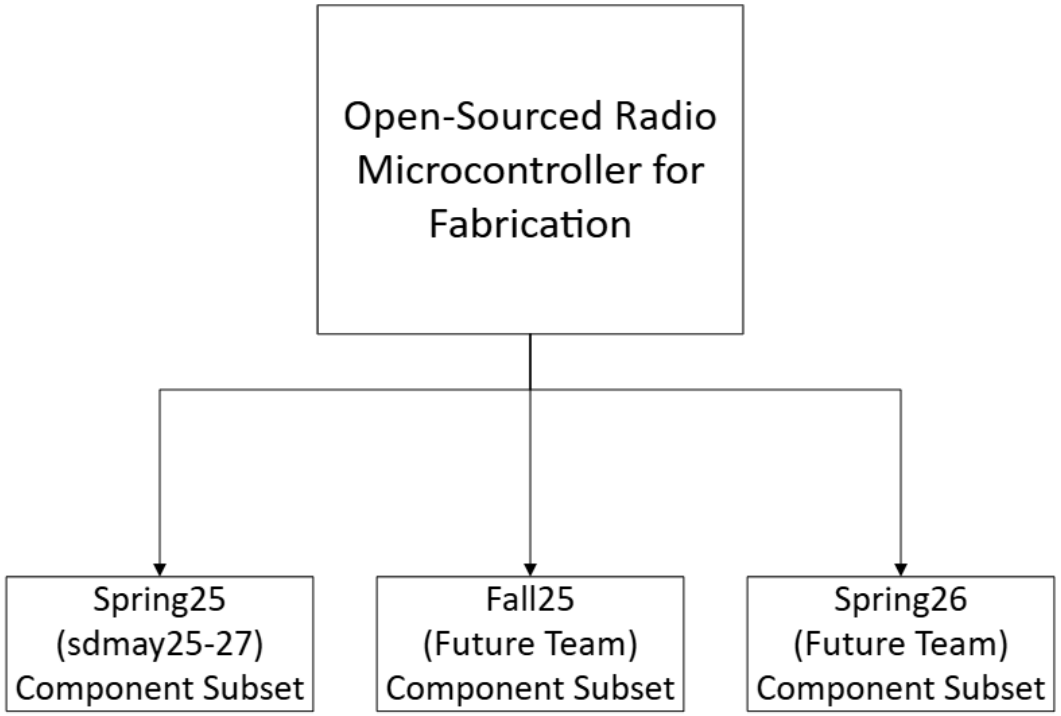
Product Services and Design	Unique Value Proposition	Product Advantages	Product Disadvantages	User Pros	User Cons
TI CC1352P  [9]	• Thread, Zigbee, Matter • Bluetooth • Low power consumption	• Low power consumption while supporting Bluetooth • Supports multiple radio protocols	Only uses 2.4GHz radio frequencies	Part of simple link system with common simple development environment	• Not open source • Designed for general use
Espressif ESP32  [1]	• Bluetooth & WIFI • Microcontroller • Multicore	• Wide variety of users • Used in low power IoT products • ESP-NOW Protocol	• Proprietary CPU architecture, limited support	• Very affordable • Easy to use libraries • Can program with Arduino IDE	• Low Range • Only • High power consumption for some peripherals
Raspberry Pi Pico W  [10]	• Wi-Fi and Bluetooth 5.2 support • PIO state machines • MicroPython support	• PIO state machines allow for flexible peripheral allocation • Dual core to allow one core to handle radio and one to handle application	264 kB memory may not be enough for some applications	• Cheap • Good documentation • No need for extra tools for programming	C/C++ SDK setup can be painful relative to other MCUs

DD 34

Potential Risks and Mitigation

Project Scope

- Risks
  - Our project is too large to for a single senior design team to complete.
- Mitigation
  - We have created a design outline for the complete project.
  - We have chosen a subset of components to implement.
  - The overall design will be considered when creating the component subset.
  - We elected not to specify the component subsets for future teams.
- DD 26



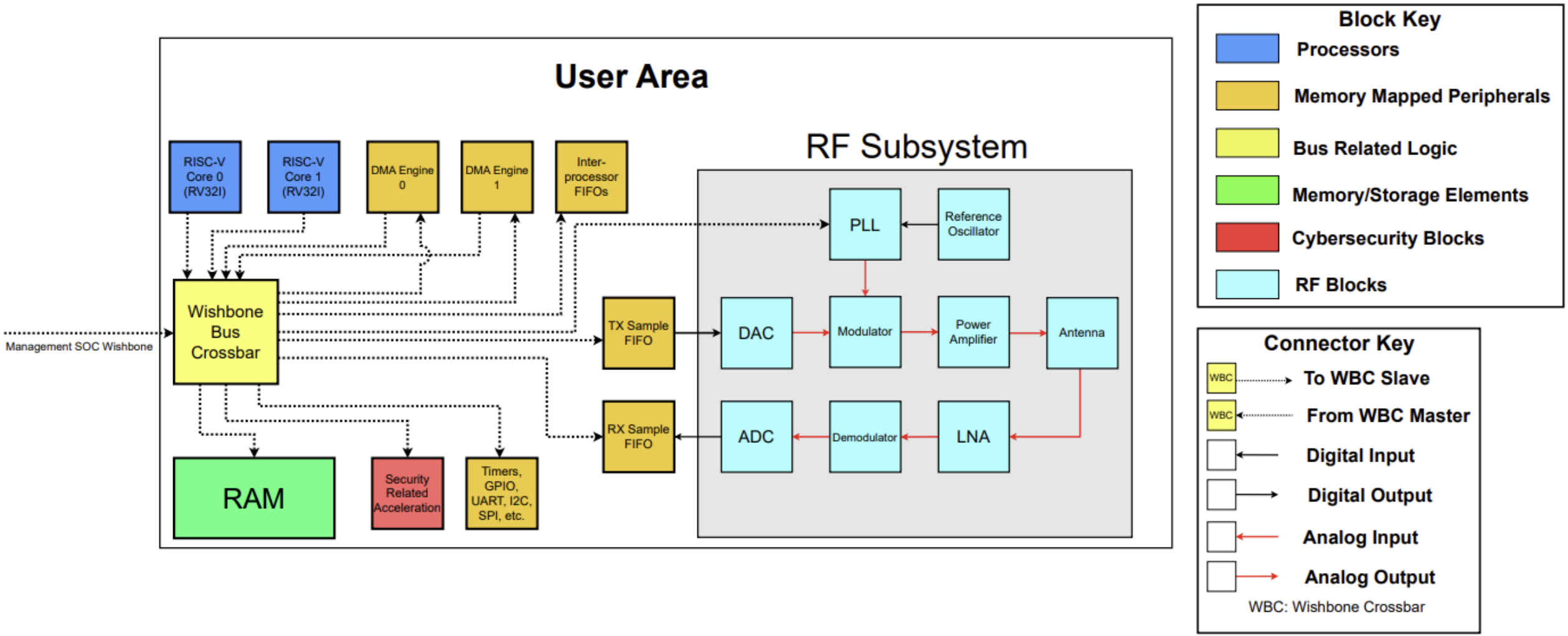
Resource/Cost Estimate

Not Provided	Cost
10MHz Crystal Oscillator	$10
Prototype PCBs	$5
Misc. Passive Circuit Components	$10
Already Provided	**Cost**
All tools and resources to develop on the Efabless platform	$0
ChipIgnite (Fabrication)	$9,750
FPGA for testing before fabrication	$300
PI Pico for testing fabricated design	$7

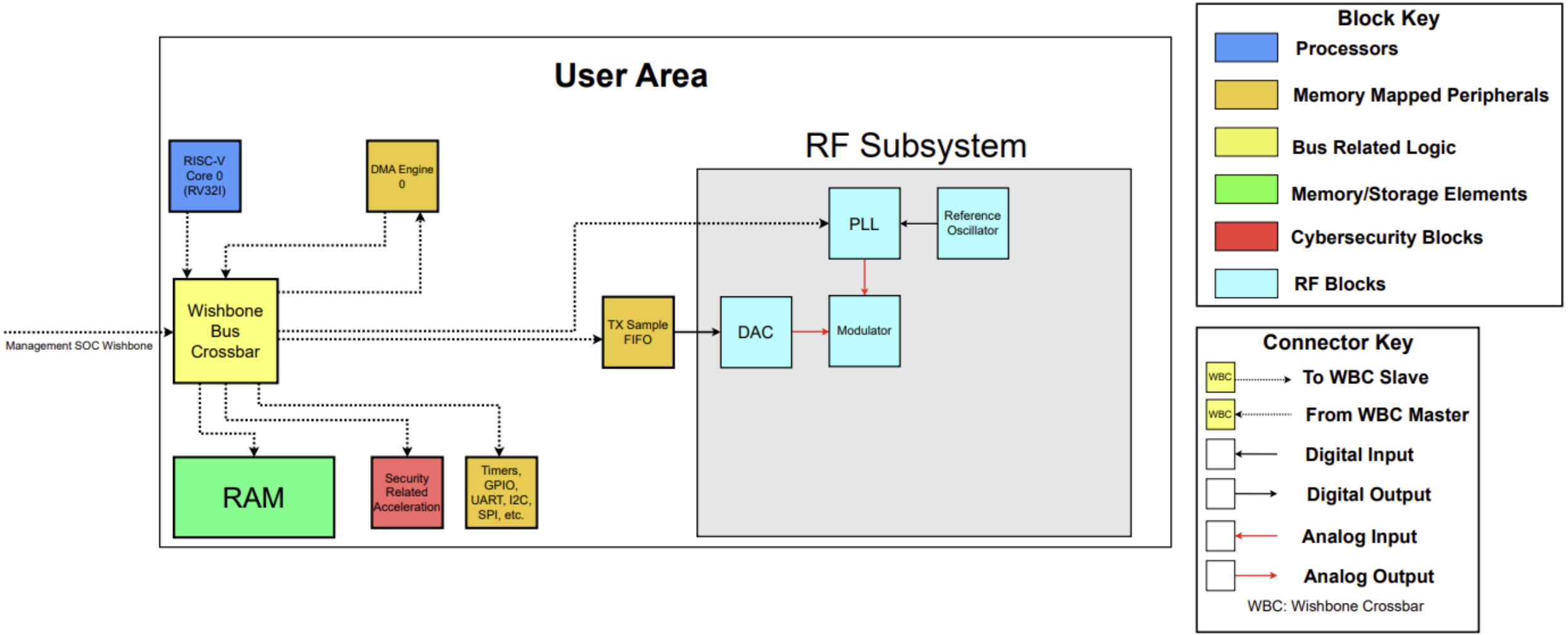
Total Cost: $10,082

All costly resources have been provided

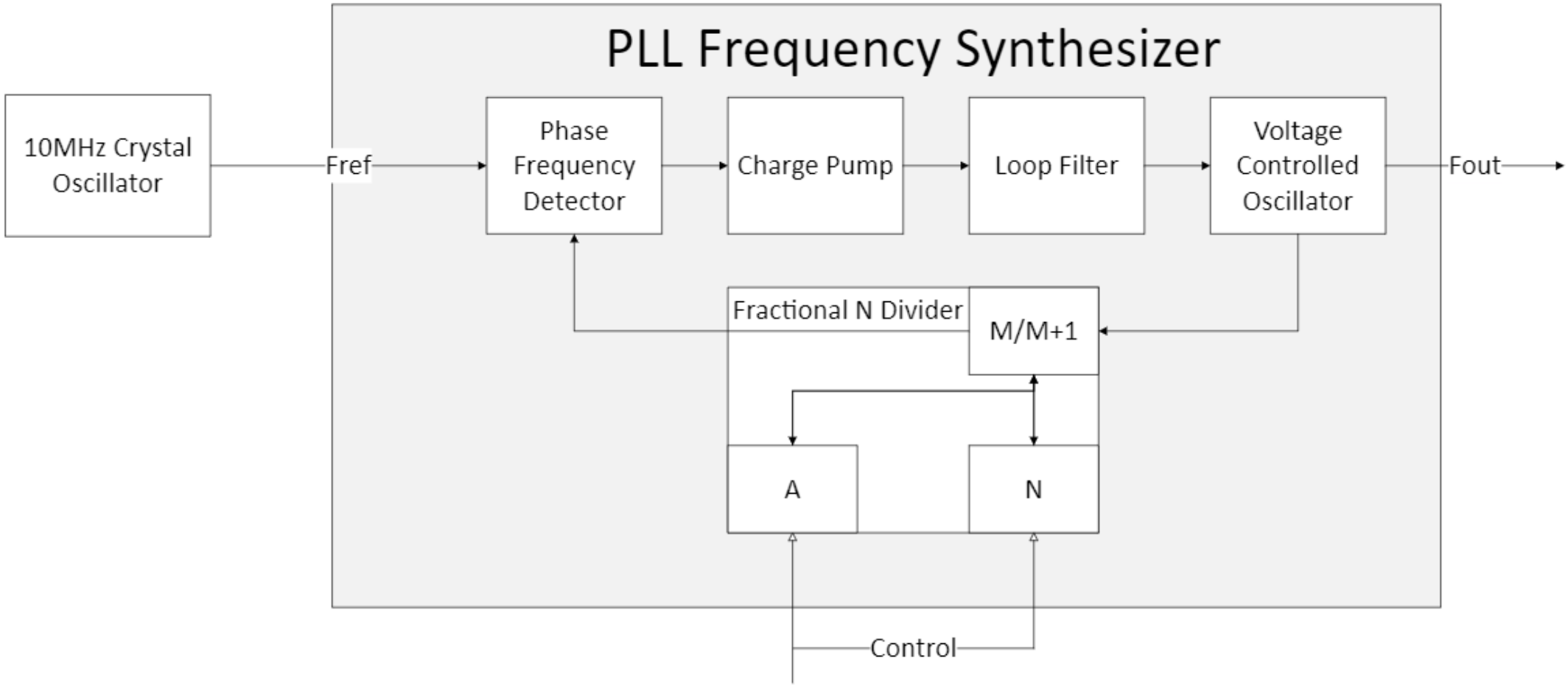
Detailed Design



Minimum Viable Product

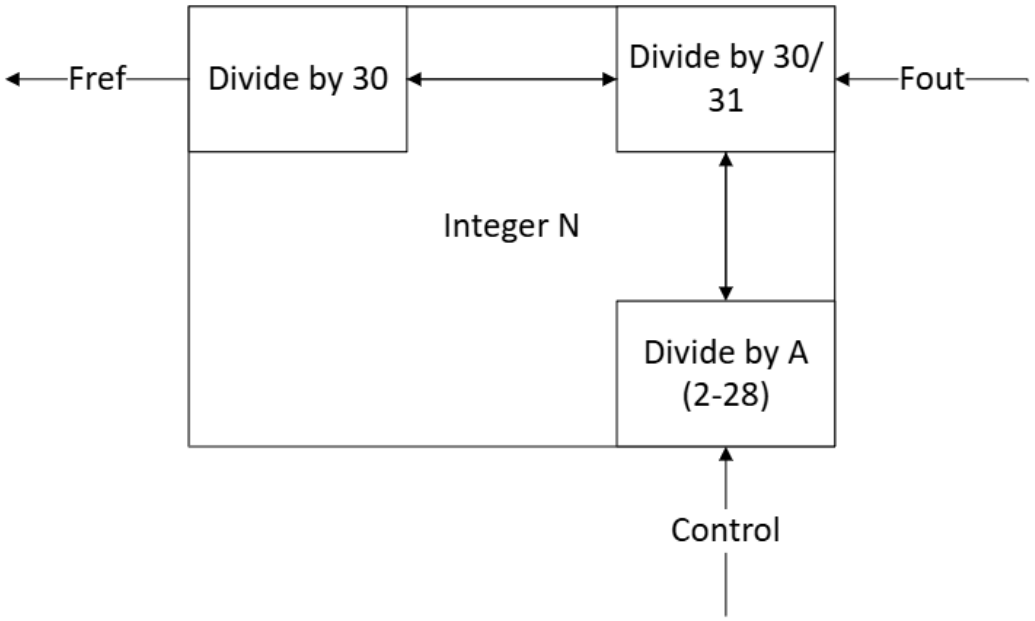


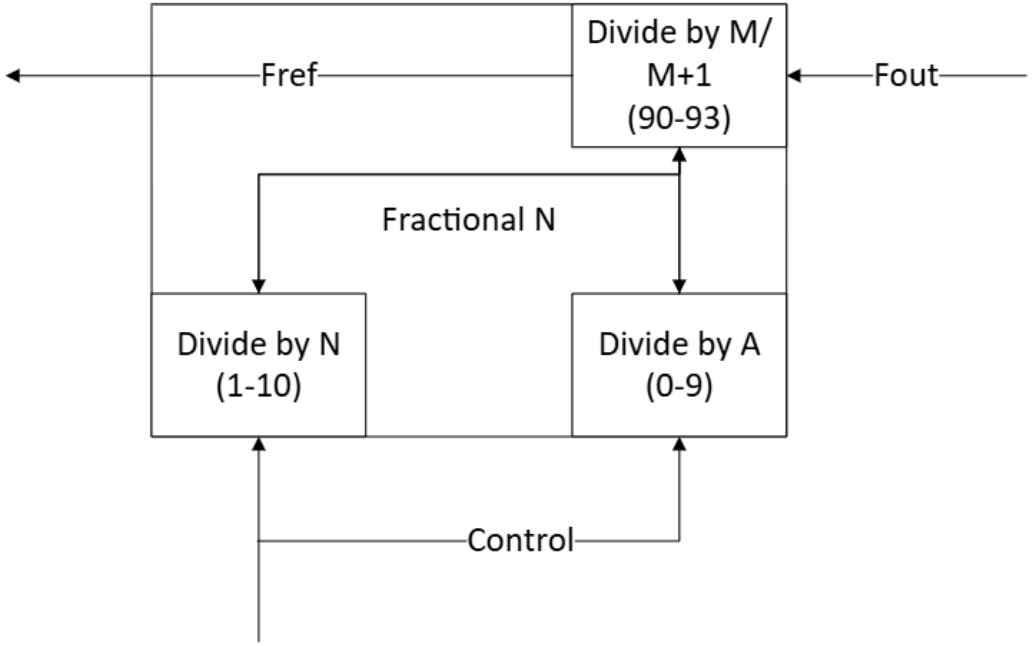
Analog PLL Design



Design Decision Example - Divider

Dual Modulus Divider	1st Order Delta Sigma Divider
Does not cause fractional Spurring	Does cause fractional Spurring
Divide by 30-31 at high frequency	Divide by 90-93 at high frequency
Reference frequency(Fref) can be 1MHz	Reference frequency(Fref) can be 10MHz





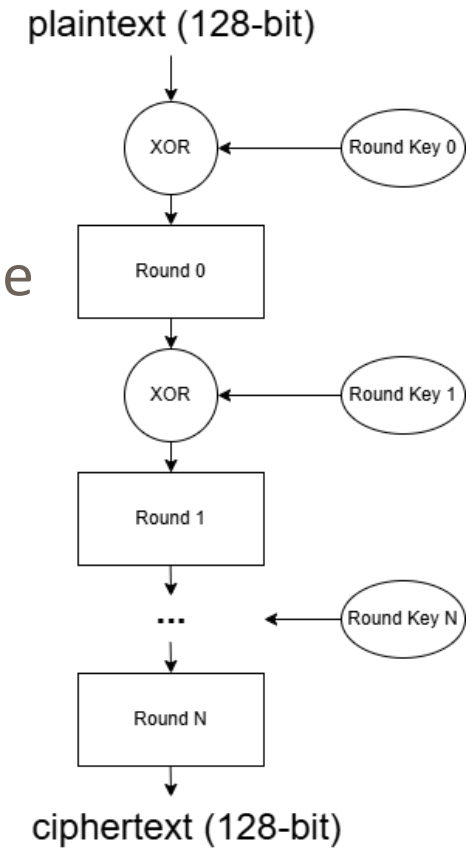
Security Analysis

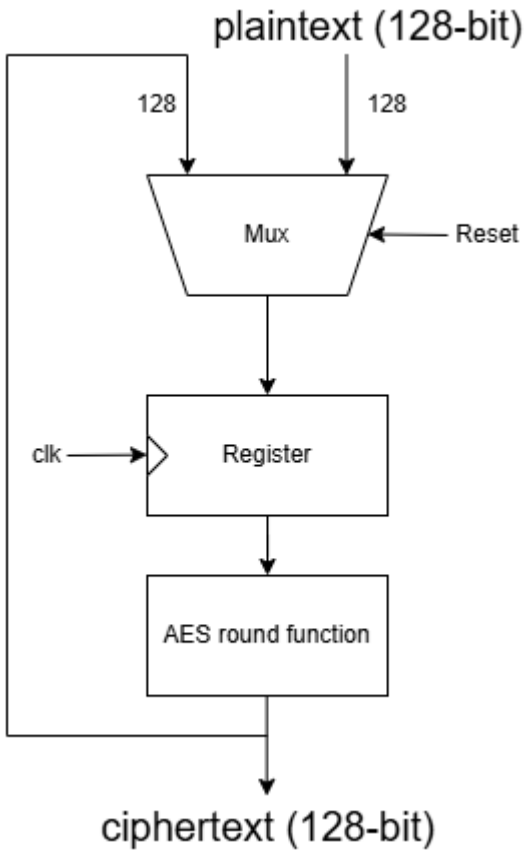
- Goal: Analyze security of the entire system, determining different possible attack vectors.
- Provide potential solutions and countermeasures for each vector.
- Determine realistic security implementations for the project.

Attack Vector	Microcontroller	Radio Frequency Module
Encryption	✓	✓
Control Flow Manipulation	✓	✓
Side-Channel Attacks	✓	
Replay Attacks		✓
E-Stop Abuse		✓
Malicious Repairing & Reprogramming		✓

Security Analysis Conclusion

- Considering the project environment and how it will be utilized, we evaluated security vulnerabilities based on levels of risk.
- Highest priority concern:
  - Encryption
  - AES Encryption based off NIST 197 Standard
  - Iterative implementation and processes with one 128-bit block at a time. (DD pg. 71.)





Technologies Used

- Skywater 130 nm process
  - Provided by Efabless
- Openlane
  - Open-source tool for hardening digital designs
- GNU Compiler Collection (GCC)
  - Compile C programs for RISC-V processors
- Spectrum Analyzer
  - For testing analog components
- Frequency Counter
  - For testing PLL input and output as well as divider output

skywater [8]

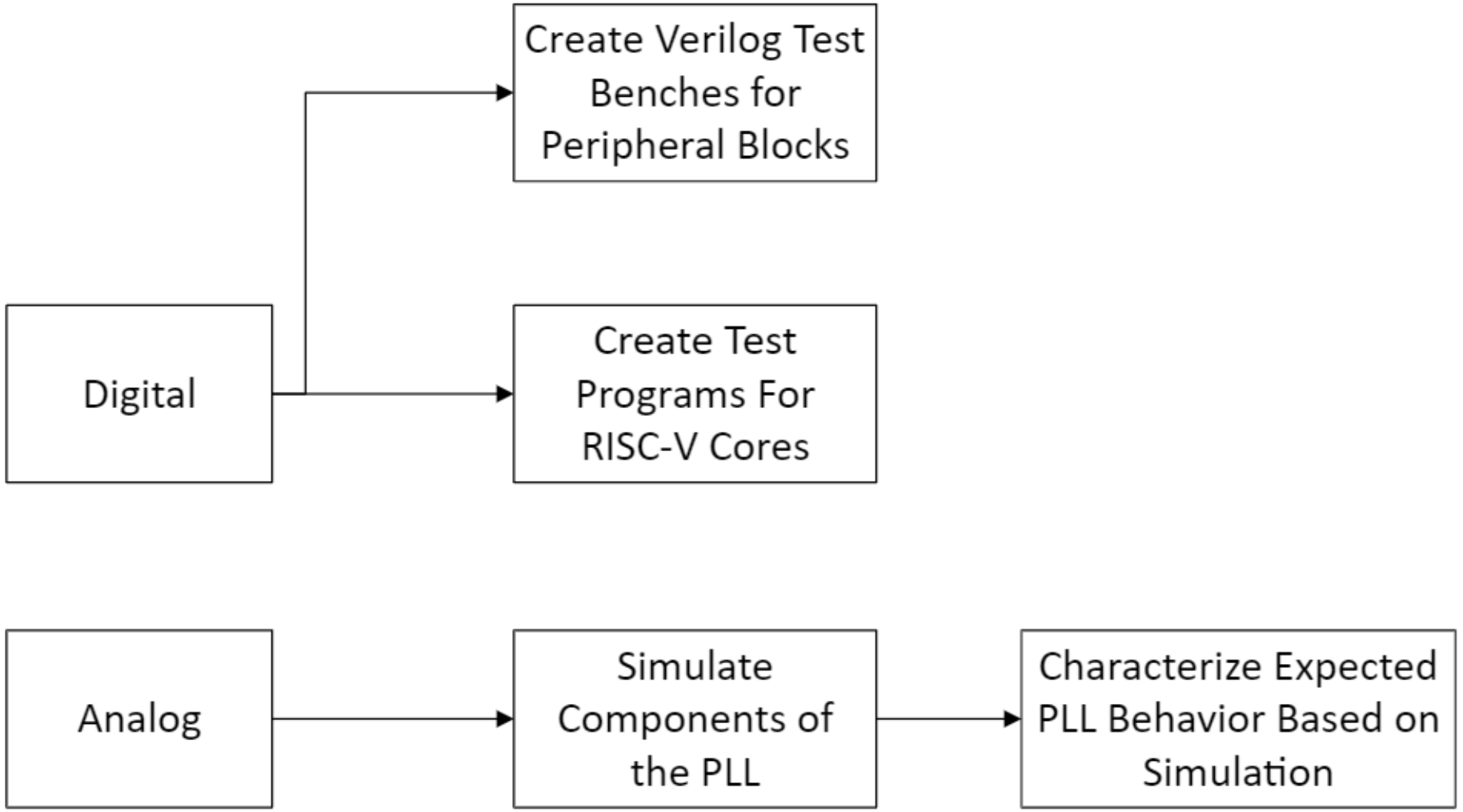
Powered by GNU [11]

[12]

[13]

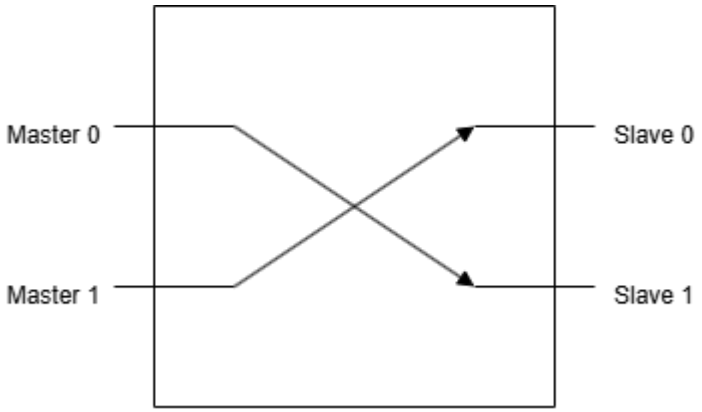
Test Plan

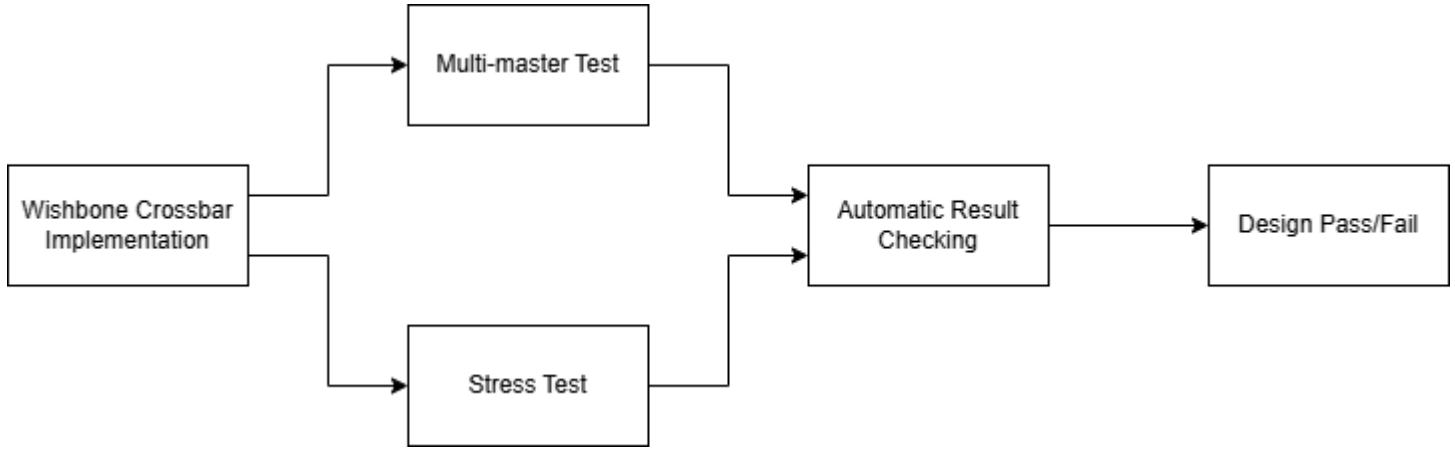
Pre-fabrication testing critical to ensure final functionality. DD 53-59



Digital Testing Example – Wishbone Crossbar

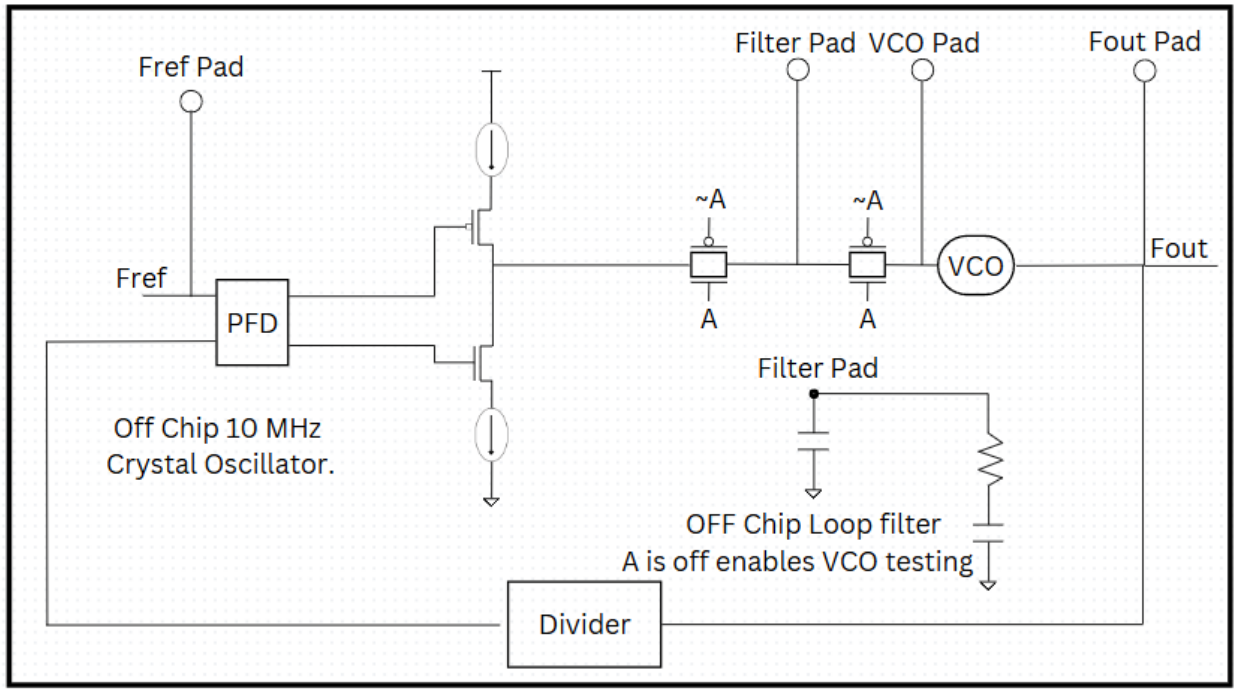
- Pre-fabrication testing will be performed using computer simulations
- Wishbone Crossbar will have two primary simulations
  - Simulate multiple masters using the crossbar simultaneously, check that requests are routed correctly and that arbitration functions properly
  - Simulate a large number (>1000) of transactions to stress test the crossbar
- Simulations can be checked automatically, providing easy verification

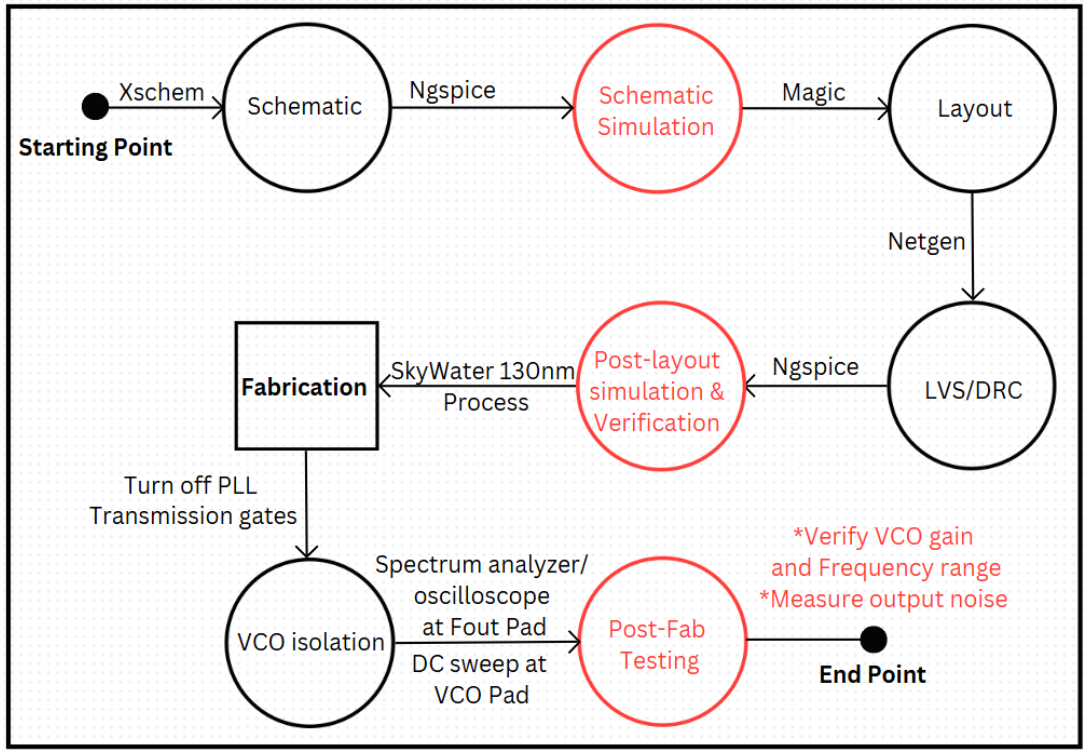




Analog Testing Example – PLL VCO

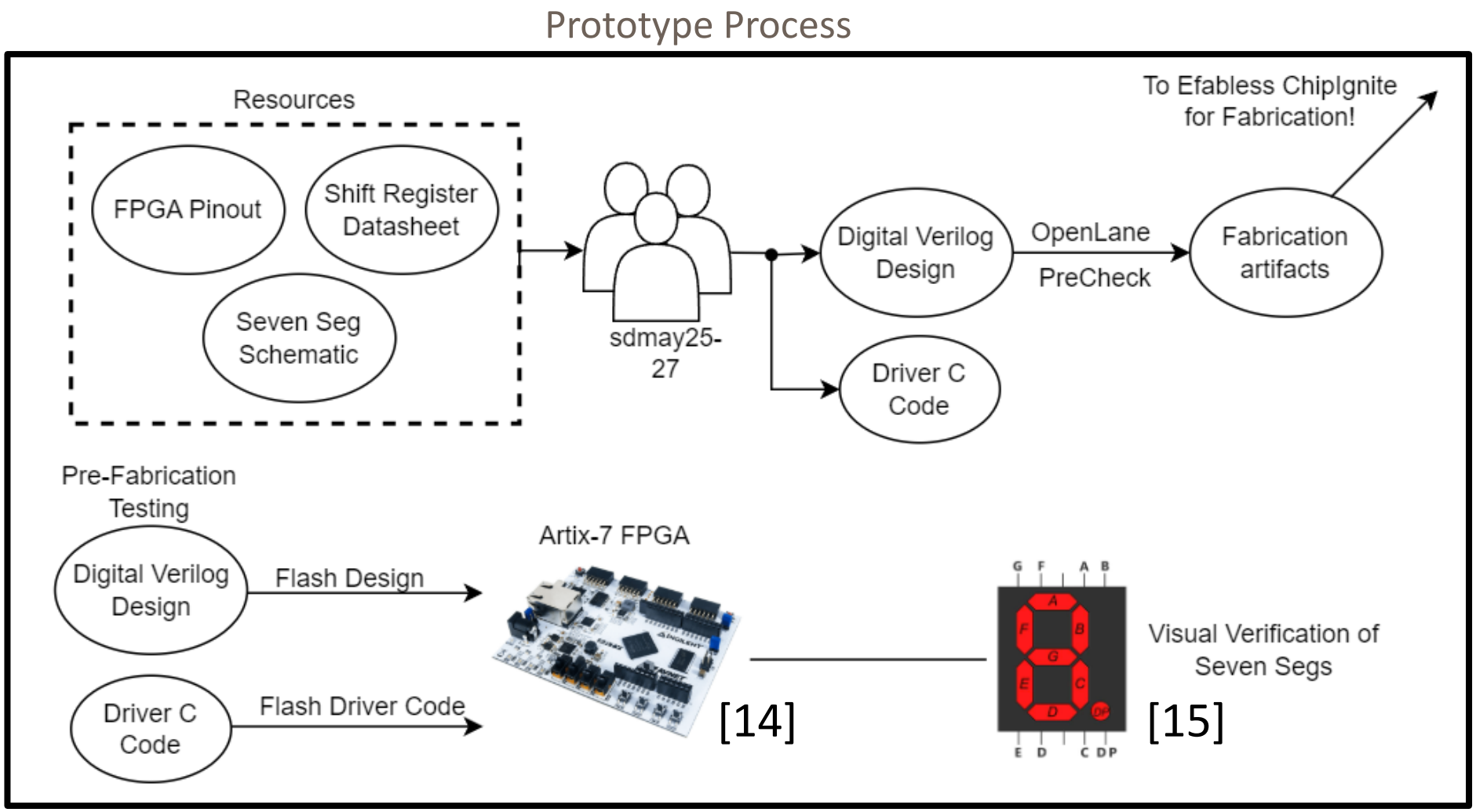
- VCO: Open Loop Configuration
  - Verify VCO gain, frequency range (0.8GHz- 1.6GHz), and output noise
    - Pre-Fabrication Testing
      - Schematic Simulation
      - Post-Layout Simulation
    - Post-fabrication Testing



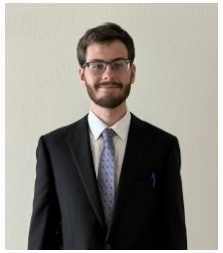


Prototype Implementations – Seven Segment Controller

- Controls two seven segments displays over a shift register interface
- Ran through OpenLane hardening and precheck
- Has been included in a chip tapeout!



Task Responsibility

	 Nathan	 Nolan	 Ibram	 Noah	 Ethan	 Will
MCU Digital Components	X	X				
Mixed Signal PLL Design			X	X		
Security Hardware and Software					X	X

Project Schedule and Key Milestones

Fall 24 Milestones	Spring 25 Milestones
Initial hardware designs finalized Specific Implementations of each PLL components Baseline implementations of peripherals RISC-V core design	Hardware components created All baseline implementations created and building
Initial test plan Defined expected behavior of each component System to test component behavior Actual designs?	Initial testing complete Hardware components tested as a system in simulation/on FPGA
	Test plan created Test cases for after fabrication to evaluate electrical characteristics and behavior of the device

Second Semester Plan

Weeks/Task		Spring 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Project Scope																	
Research available tools	OpenRAM																
	RISC-V Core Generation																
Wishbone Crossbar Creation																	
RISC-V Core Creation																	
SRAM Generation																	
DMA Controller																	
Security Component	AES 128-bit Encryption																
External Peripherals																	
Fabrication																	
Post Fabrication Test Design																	
Radio Frequency Components	Bluetooth																
	ZigBee																
Phase Locked Loop (PLL)	Research																
	Phase Frequency Detector																
	Charge Pump																
	low Pass Filter																
	Voltage Controlled Oscilator																
	Divider																
	Testing																
Create Design Documents																	
Create Testing Documents																	
Testbench Creation	Peripherals																
	RISC-V Core																

Key:

- Initial Design
- Research
- Implementation
- Fabrication

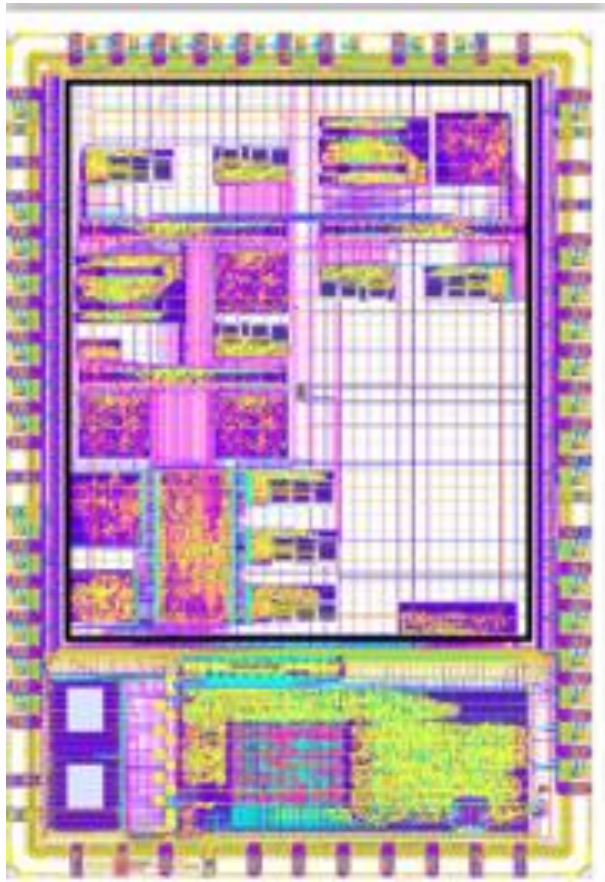
Current Status

- The tool flow provided by Efabless and ChipForge has been studied and used in example projects
- Prototype for the Wishbone crossbar has been created
- Some example RISC-V cores have been generated
- High-level designs for the digital and analog parts of the design have been created
- Substantial research for the PLL have been done
- The design document has been finished

Conclusion

- We have used this semester to scope the project to fit our team's abilities
- We have designed components that, based on our research, will meet our project requirements
- We have learned how to use the Efabless process to design components
- We have created a test plan to be confident in the viability of our designs prior to tape-out

TAPEOUT!



[7]

Questions?

ECPE Senior Design May 2025, Team 27

Image References

[1] ESP 32: https://mm.digikey.com/Volume0/opasdata/d220001/medias/images/425/MFG_ESP32-DEVKITC-VE.jpg

[2] STM: https://newsroom.st.com/wp-content/uploads/2020/12/STM32WL_MM_launch_P4314S_big.jpg

[3] PI Pico: https://cdn-shop.adafruit.com/970x728/5544-02.jpg

[4] Generic Microcontroller: https://www.electronics-lab.com/top-10-popular-microcontrollers-among-makers/

[5] Wifi Waves: https://www.vecteezy.com/free-vector/wifi-waves

[6] Chip Forge Logo: https://git.ece.iastate.edu/isu-chip-fab

[7] Caravel Diagram: https://efabless.com/open_shuttle_program

[8] Skywater: https://www.skywatertechnology.com/wp-content/uploads/2024/01/MicrosoftTeams-image-5.jpg

[9] TI CC1352P: https://www.ti.com/product/CC1352P

[10] Raspberry PI Pico: https://www.allaboutcircuits.com/news/at-just-six-dollars-raspberry-pi-pico-w-brings-wi-fi-to-iot-designs/

[11] GNU Logo: https://worldvectorlogo.com/logo/gnu-4

[12] Spectrum Analyzer: https://siglentna.com/spectrum-analyzers/ssa3000x-plus/

[13] Frequency Counter: https://www.keysight.com/us/en/product/53131A/225-mhz-universal-frequency-countertimer.html

[14] FPGA: https://cdn11.bigcommerce.com/s-7gavg/images/stencil/1280x1280/products/471/3908/Arty_obl_2_600__25304.1670980518.png?c=2

[15] Seven Seg: https://softwareparticles.com/wp-content/uploads/2023/04/7seg-led-display-pintout-1.jpg