

The background of the slide is a dark, moody image of a stormy sky. Several bright, jagged lightning bolts are visible, with one prominent bolt striking down from the upper right towards the center. The clouds are dark and textured, creating a sense of depth and drama.

# Detailed Design Lightning Talk

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Nathan Stark, Nolan Eastburn, Noah Thompson, Will Custis, Ethan Kono, Ibram Shenouda

Client/Advisor: Dr. Duwe

# Project Overview

- Design a microcontroller with radio communication capabilities
- Open-source
- Can be fabricated
- Will be used by ISU ChipForge group, possibly faculty and hobbyists
- Designed using the Caravel platform from Efabless
- Inspired by the TI CC1352P (block diagram shown to the right)

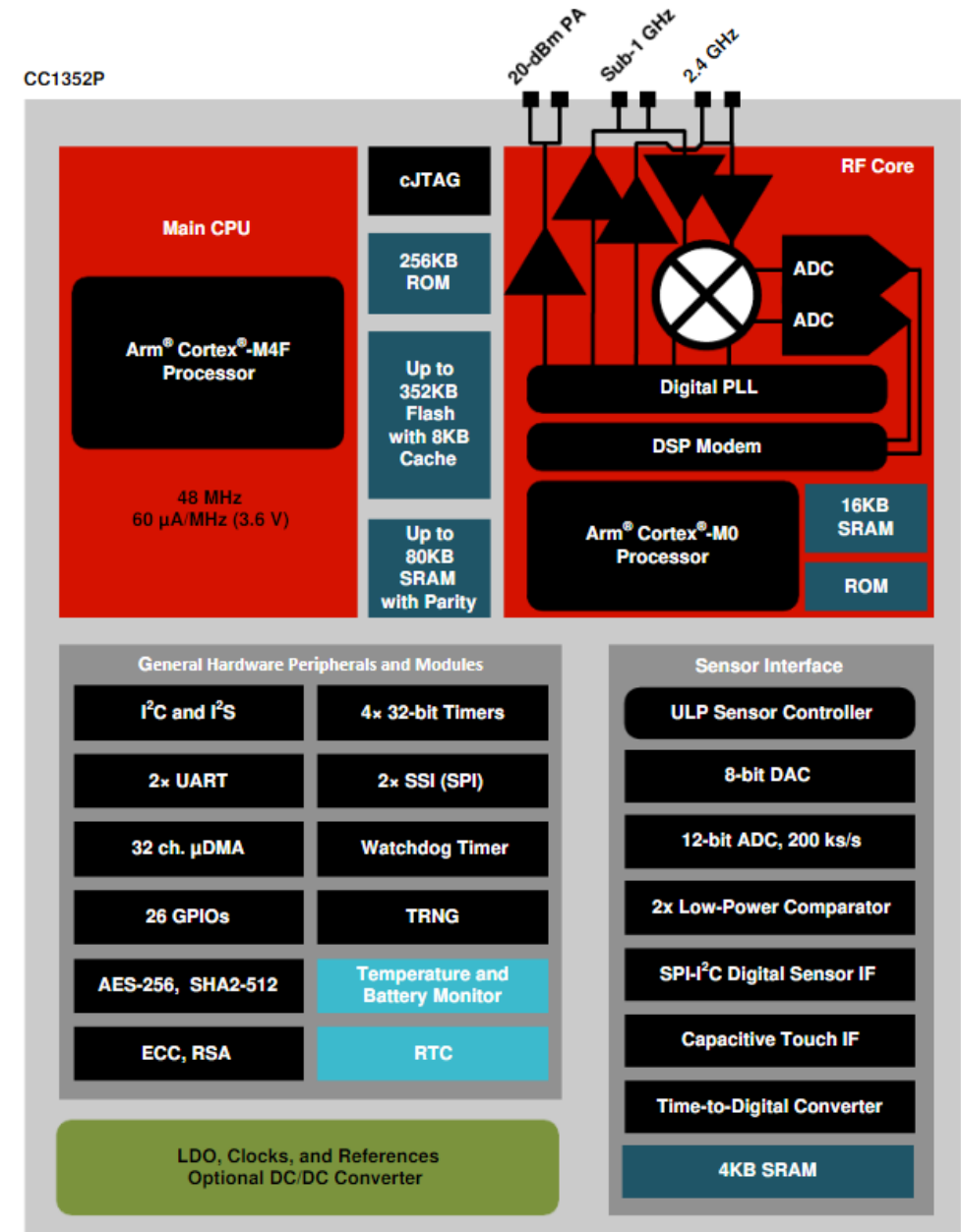
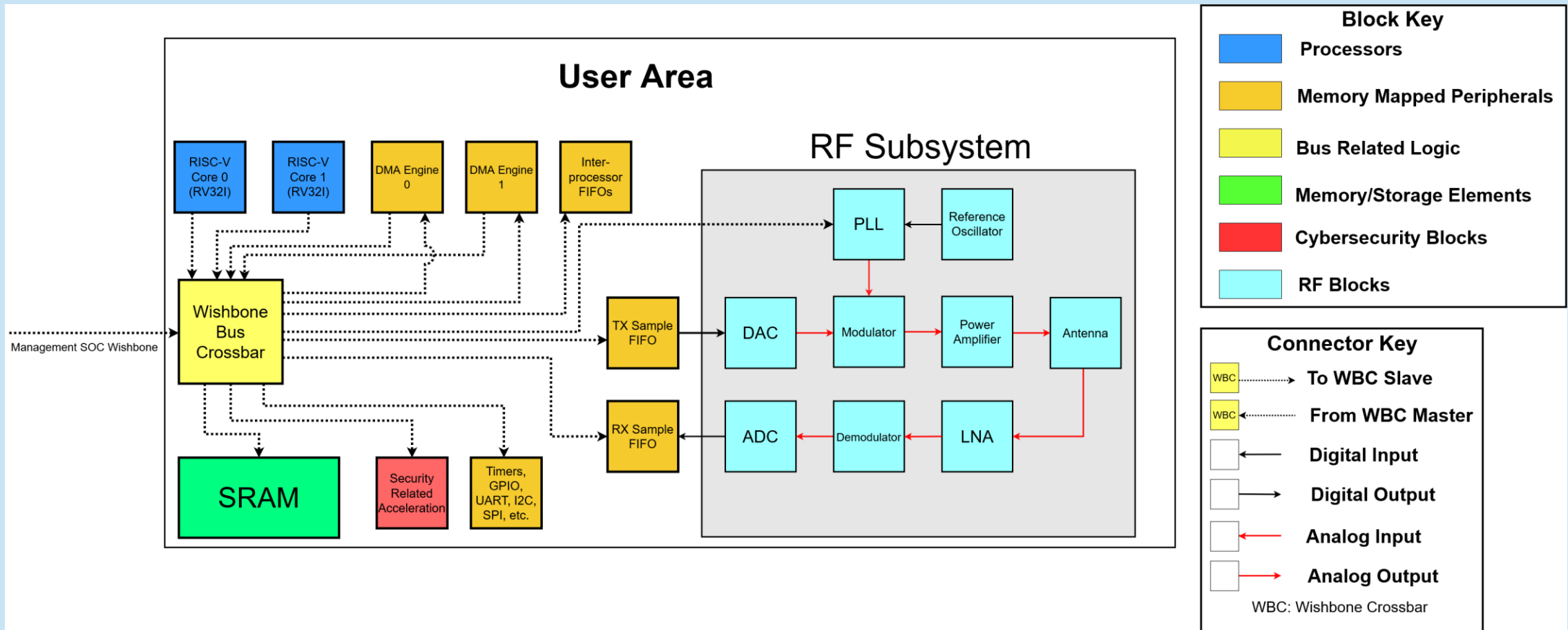
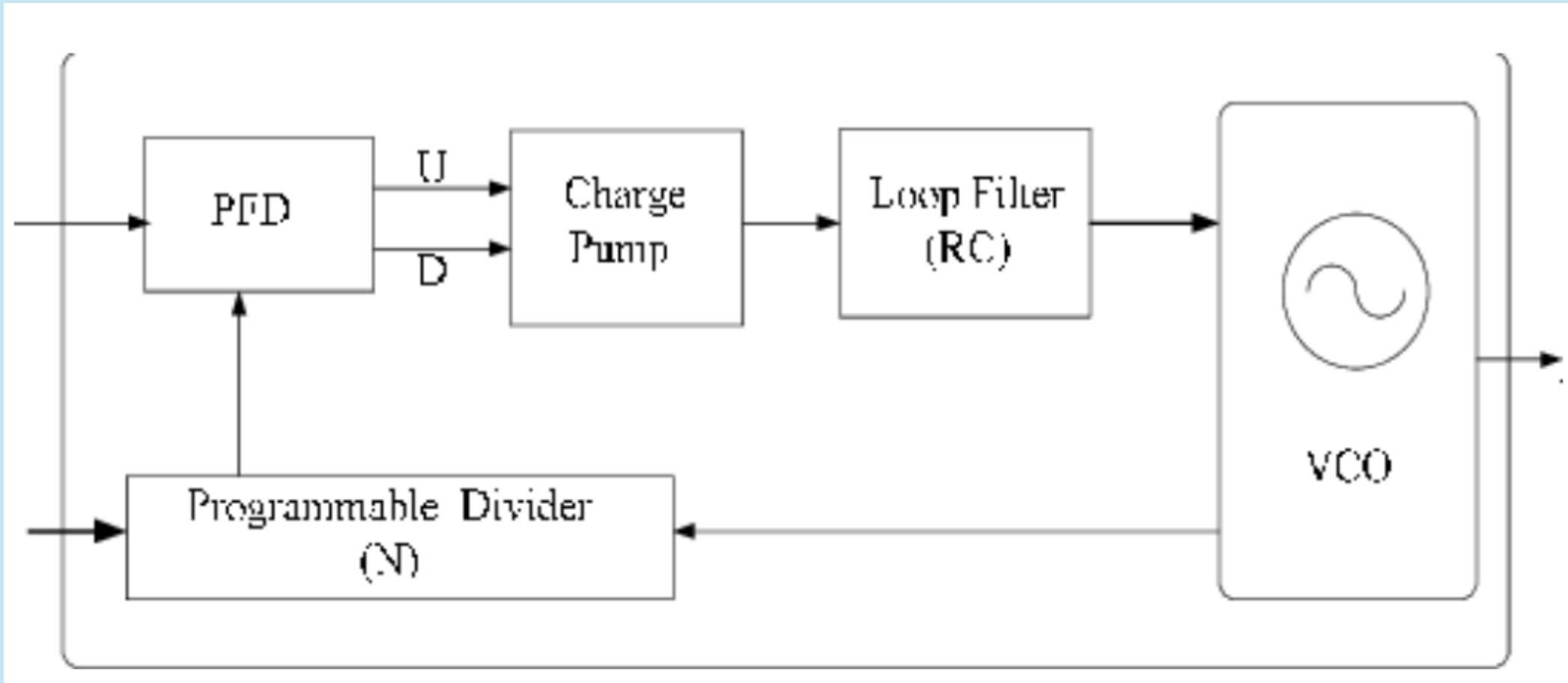


Figure 4-1. CC1352P Block Diagram

# Detailed Design – Block Diagram



# Detailed Design – PLL



# Functionality – Basic Use Case

- Users will write C programs for their specific application
- Application will be compiled and uploaded to the microcontroller using a PC
- Processor running application can communicate with other devices using Zigbee standard
- Other peripherals, such as DMA, UART, I2C, or SPI provide additional capabilities to user applications to interact with devices or offload operations from the processor

# Technology Considerations - Pros

- Efabless Skywater 130nm Process
  - Cheap initial manufacturing cost
    - ~\$10000 vs > \$1 million for modern processes
  - Built-in debug functionality outside user design
- Open-source Efabless Tools
  - Free and easily available
  - Proven to work with Efabless process

# Technology Considerations - Cons

- Efabless Skywater 130nm Process
  - Older process
  - Limited RAM capacity, slower clock speeds
- Open-source Efabless Tools
  - Tooling support is less sophisticated than paid tools
    - More difficult to get desired behavior
  - Learning curve due to lack of experience
  - Documentation sometimes out of date or lacking information
  - Analog design particularly difficult

# Technology Considerations - Solutions

- No alternatives available
  - Required to use these by client
- Efabless Skywater 130nm Process
  - Carefully size RAMs and peripherals to minimize usage
  - May have to make area vs speed tradeoffs
- Open-source Efabless Tools
  - Fail early, fail often
    - Don't want to wait until last minute to try and run design through
  - Talk to people with prior experience



# Areas of Concern and Development

- Unclear if necessary functions will even be possible in technology
  - Part of the project is to evaluate this
  - Will be difficult to tell until much of design created
- Project will be multi-part, our group is only implementing a portion of the design
  - Not all components users may need will be finished
  - Our minimum product will provide many features and allow evaluation of whether rest of project is viable

# Conclusion

- Early work with the design tools will be critical to success
- Process constraints may reduce performance or functionality
  - May need to cut one or the other
  - Currently difficult to predict due to little being implemented
- Process has potential to make this a low-cost solution