Project Planning Lightning Talk

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Client/Advisor: Dr. Duwe

Project Overview

- Design a microcontroller with radio communication capabilities
- Open-source
- Can be fabricated
- Will be used by ISU ChipForge group, possibly faculty and hobbyists
- Designed using the Caravel platform from Efabless
- Inspired by the TI CC1352P (block diagram shown to the right)

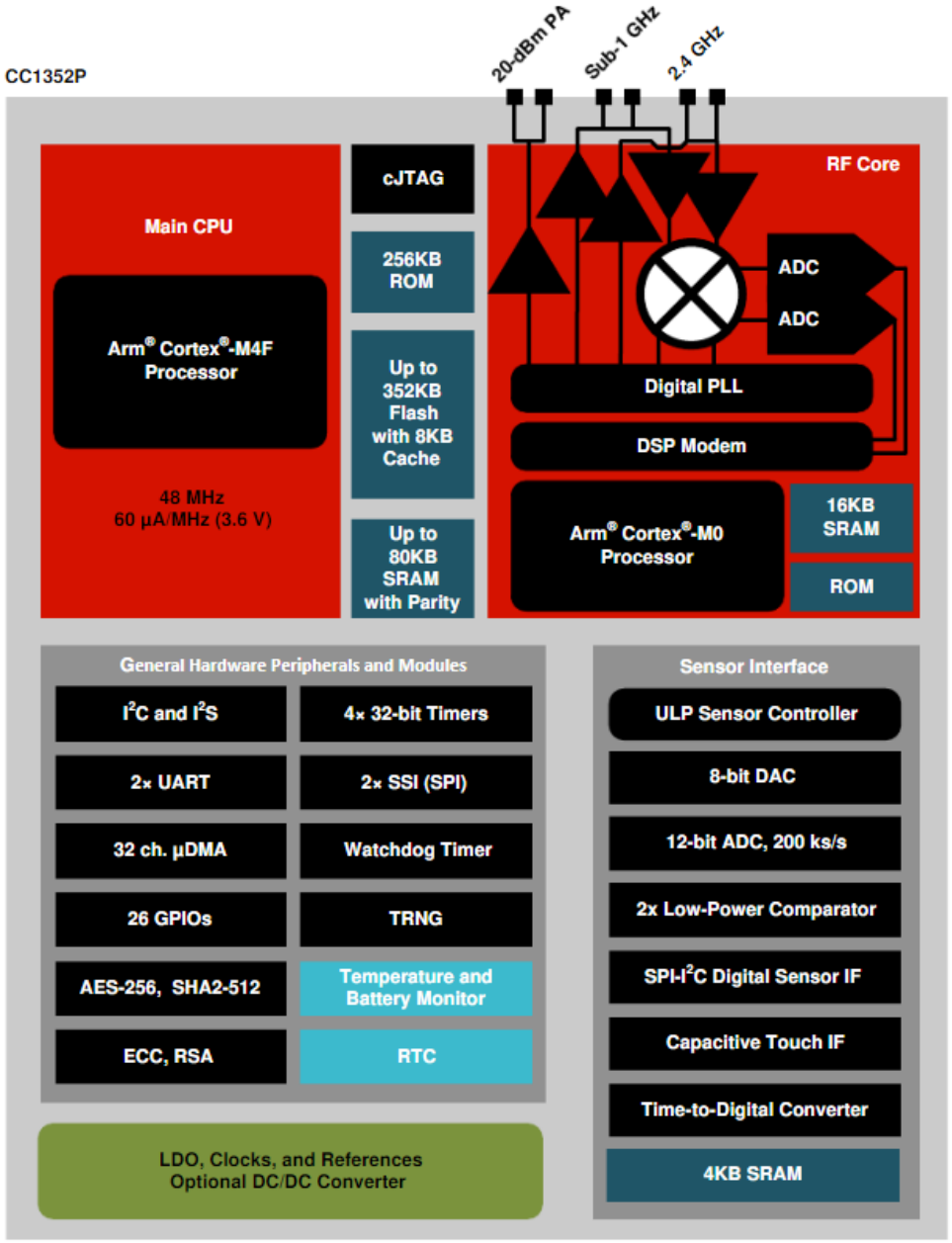
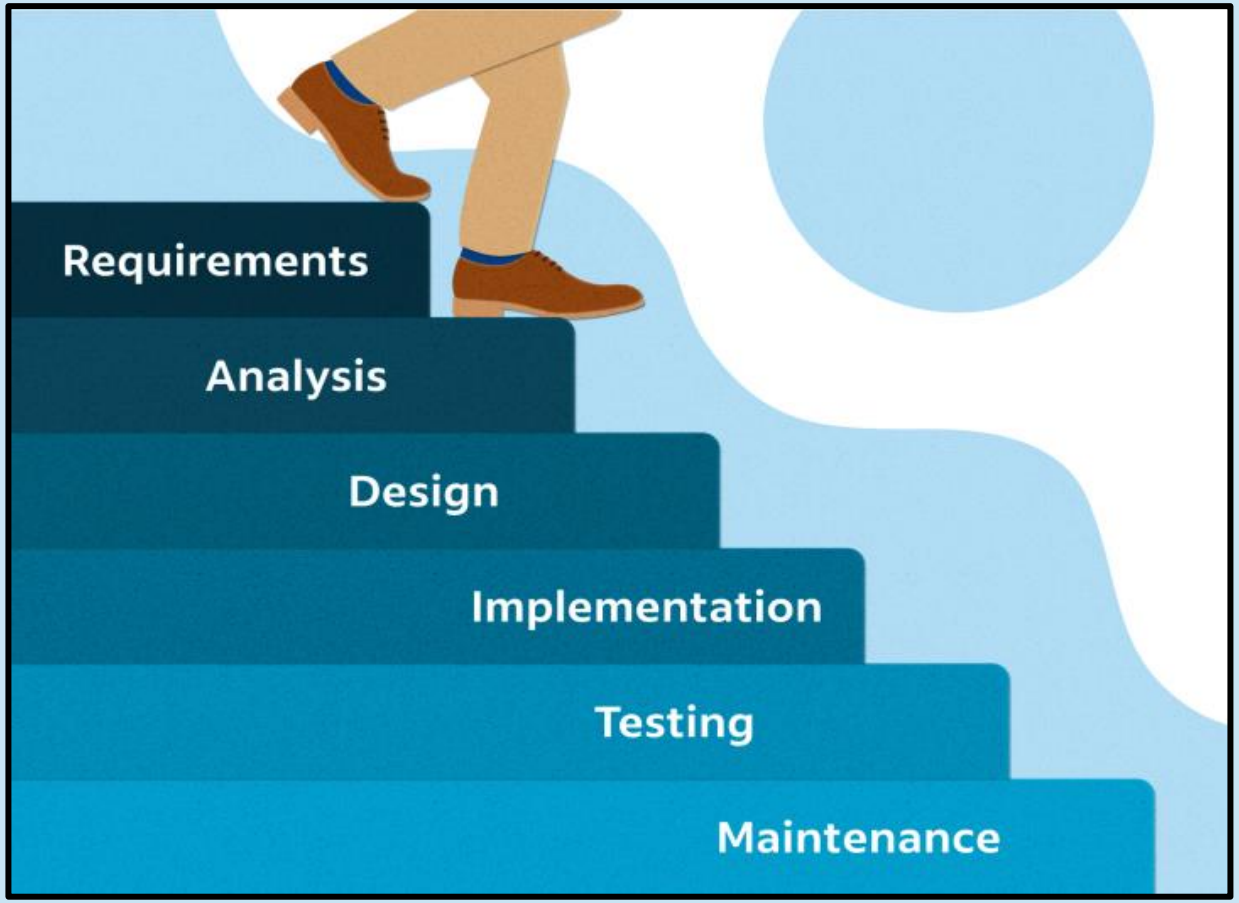


Figure 4-1. CC1352P Block Diagram

Image Source: https://www.ti.com/lit/ds/symlink/cc1352p.pdf?ts=1727935470469&ref_url=https%253A%252F%252Fwww.mouser.es%252F

Project Management Style

- Using a Waterfall approach
- Useful since project has a small set of large deliverables
- Challenging to do incremental development using Agile with so many interconnected components



Waterfall Image Source: https://images.ctfassets.net/pdf29us7flmy/1emIth09wz9enIMbENOewu/5445d327ac12235558850ed25b0662eb/-IND-004-049-_Waterfall_Methodology_Final.jpg?w=720&q=100&fm=jpg

Task Decomposition

- Four primary categories
  - Documents
    - Design document
    - Test plan document
  - Hardware Implementation
    - Digital components
    - Analog components
  - Software Implementation
    - Zigbee protocol
    - Flash application
    - Firmware
  - Testing
    - Digital simulation
    - Test programs
    - Analog simulation

1 of 3 of our task decomposition graphics

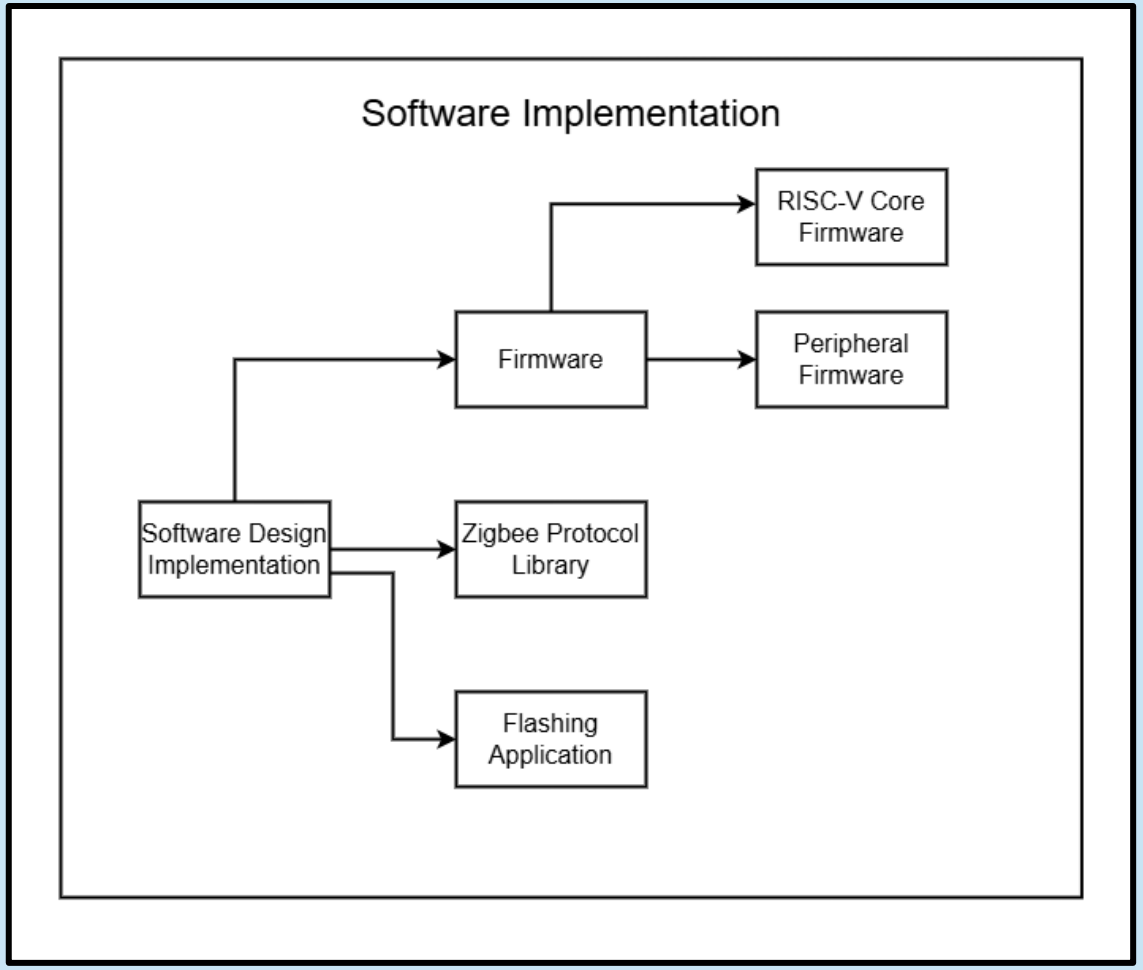
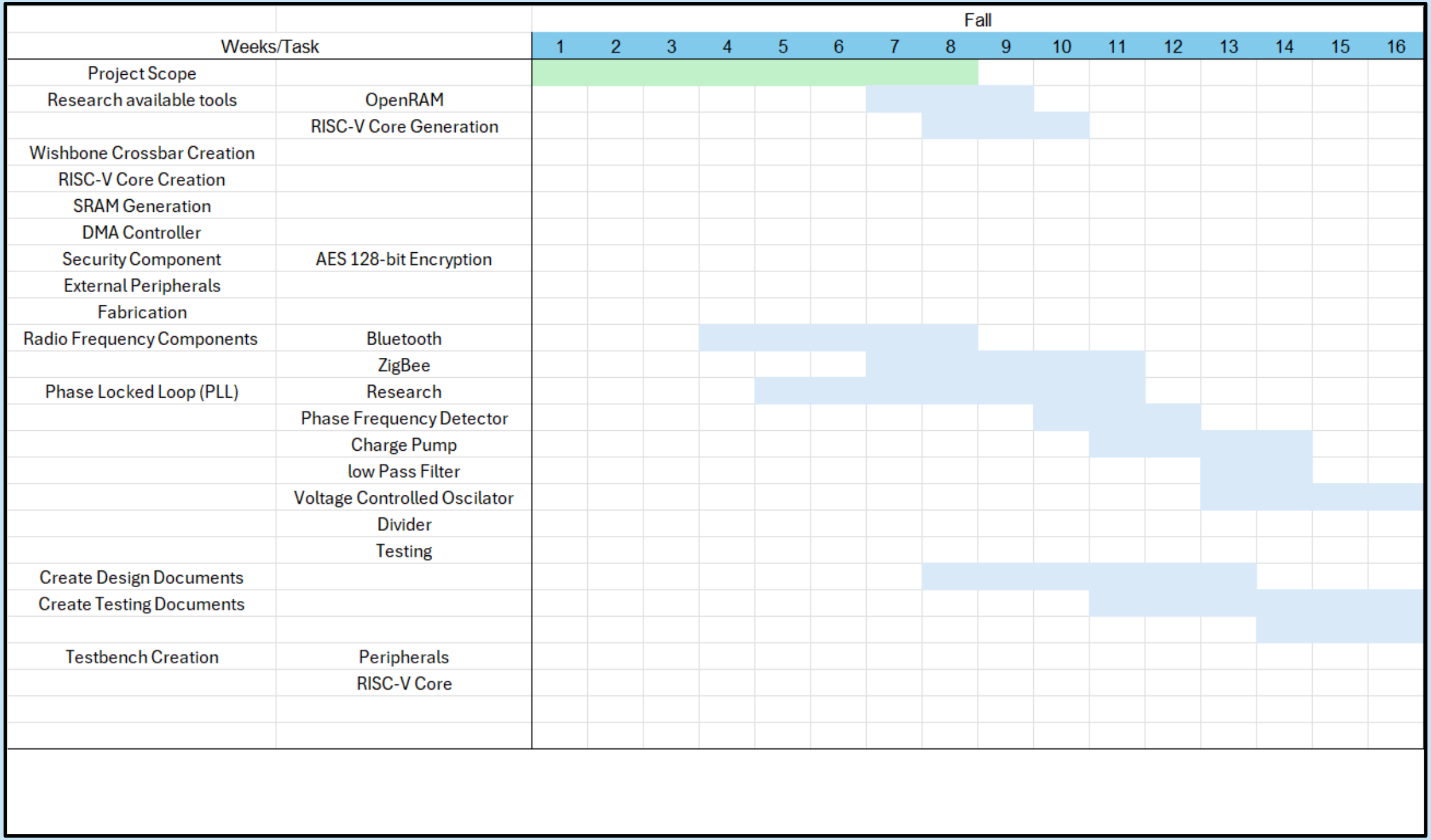


Image Source: Created by our team.

Key Milestones and Metrics

- Design document finished
- Hardware components created
  - All baseline implementations created and building
- Initial testing complete
  - Hardware components tested as a system in simulation/on FPGA
- Test plan created
  - Test cases for after fabrication to evaluate electrical characteristics and behavior of the device
  - Test cases should cover all peripherals and electrical characteristics

Gantt chart for fall period on the next slide


Fall
Weeks/Task
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Project Scope
Research available tools
OpenRAM
RISC-V Core Generation
Wishbone Crossbar Creation
RISC-V Core Creation
SRAM Generation
DMA Controller
Security Component
AES 128-bit Encryption
External Peripherals
Fabrication
Radio Frequency Components
Bluetooth
ZigBee
Phase Locked Loop (PLL)
Research
Phase Frequency Detector
Charge Pump
low Pass Filter
Voltage Controlled Oscilator
Divider
Testing
Create Design Documents
Create Testing Documents
Testbench Creation
Peripherals
RISC-V Core

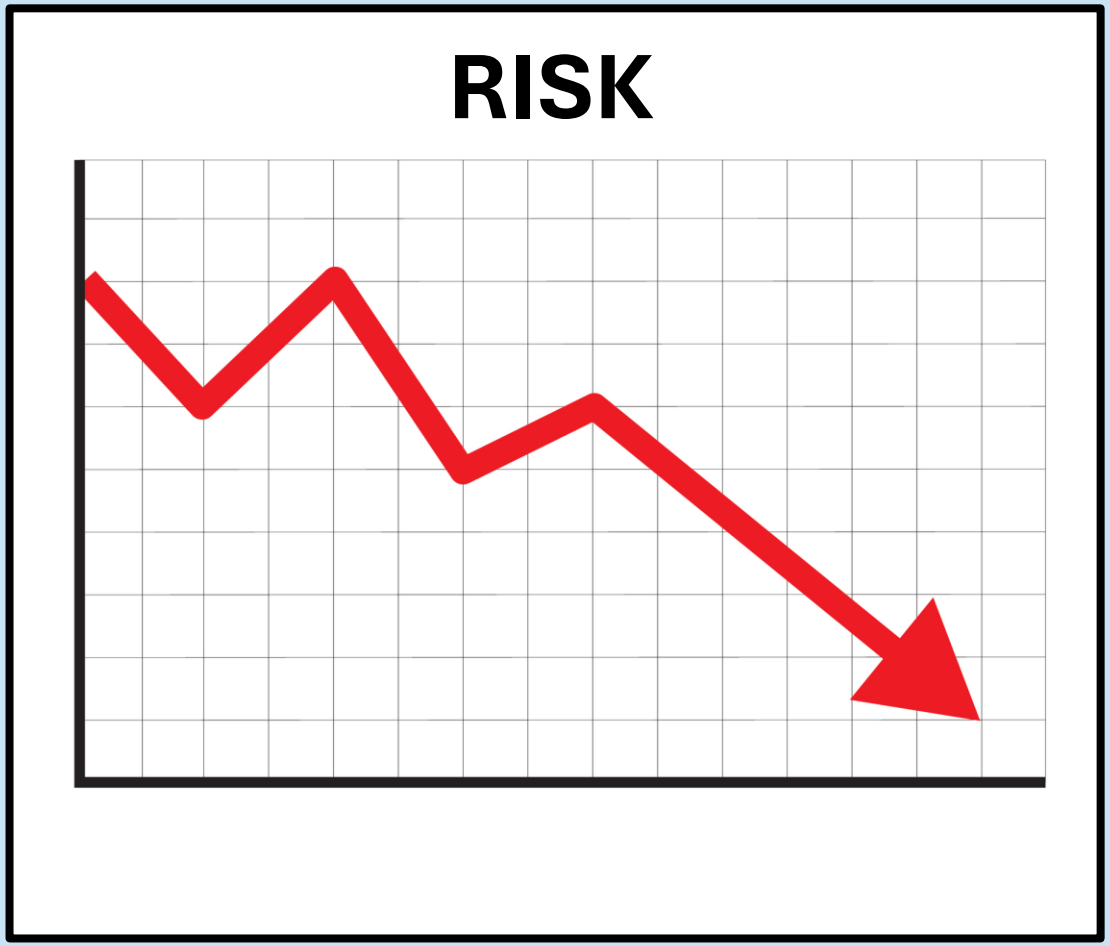
Key Risks

- Unknown design tools
  - Design tools are different from those used in ISU courses
  - Some tools have known issues that may cause delays
- Limited die space (2.92 mm x 3.52 mm)
  - May not be possible to fit everything we want
  - Difficult to evaluate prior to initial implementation

Caution Image Source: https://static.vecteezy.com/system/resources/previews/015/309/552/non_2x/warning-caution-sign-on-transparent-background-free-png.png

Risk Mitigation

- Unknown design tools
  - Currently working to get acquainted with tools
  - Dr. Duwe has pointed us towards some people who have more experience with tools
- Limited die space
  - Have created list of components in minimum viable product
  - If die space becomes issue, can strip out components incrementally



Down Arrow Source: https://g.foolcdn.com/editorial/images/778429/1-simple-red-arrow-declining-stock-chart-on-a-white-checked-background.jpg

Conclusion

- There are four primary tasks to complete for the project
- Tasks are somewhat dependent on each other
  - Will require good coordination to stay on schedule
- Risks associated with unfamiliar tools and process limitations
  - Doing more research to understand, have options to reduce impact