Prototyping

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Client/Advisor: Dr. Duwe

Project Overview

- Design a microcontroller with radio communication capabilities
- Open-source
- Can be fabricated
- Will be used by ISU ChipForge group, possibly faculty and hobbyists
- Designed using the Caravel platform from Efabless

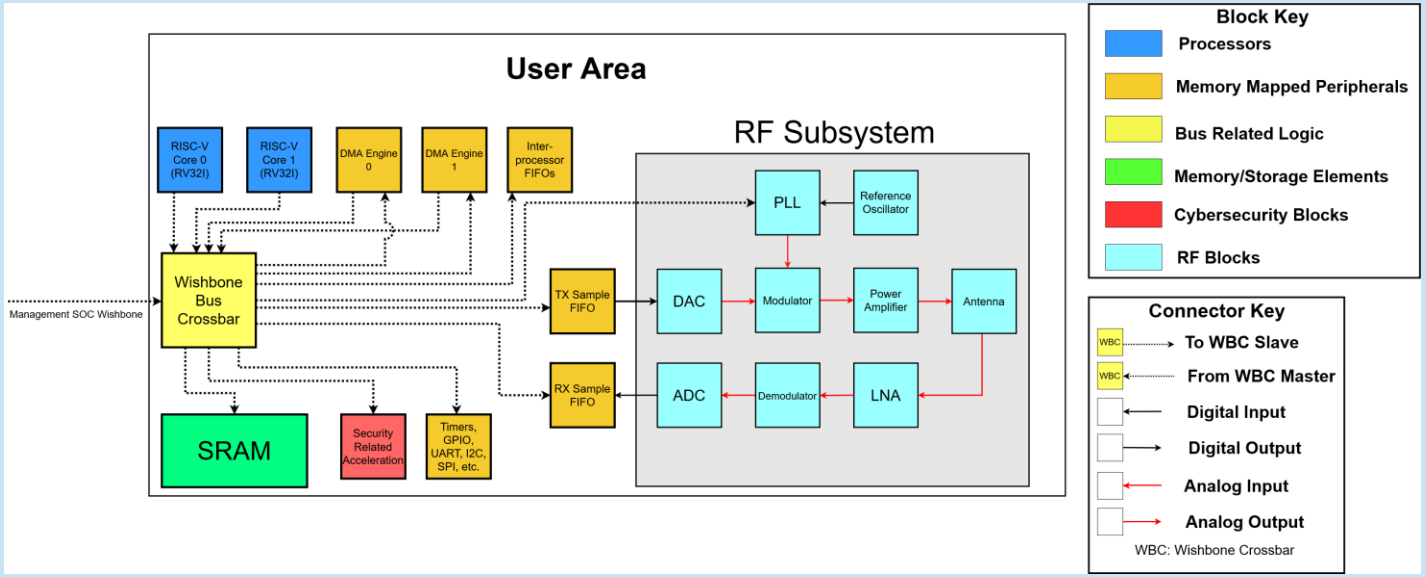
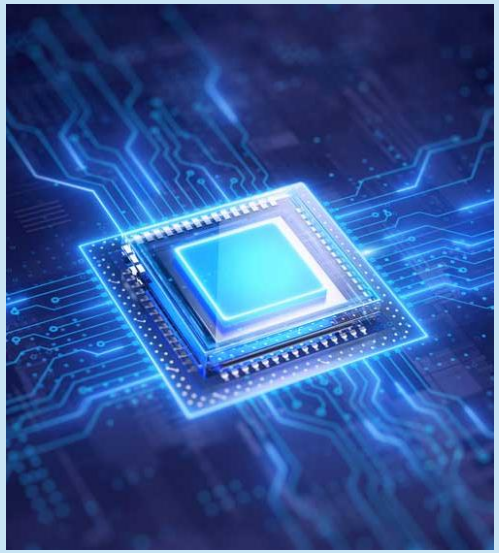


Image Source: Created by our team

Wishbone Crossbar Prototype

- Wishbone is a bus protocol used to connect a processor to various peripherals
  - RAM, UART, Accelerators, etc
- Crossbar useful to arbitrate access to peripherals without restricting throughput
- Current iteration is 2x2
  - 2 Wishbone Master Interfaces
  - 2 Wishbone Slave Interfaces
  - Any master can access any slave, provided nothing else is accessing the slave simultaneously
- Current iteration appears to function correctly
  - Need to expand to make crossbar generic



CPU Bus: https://www.wellpcb.com/wp-content/uploads/2023/01/2.jpg

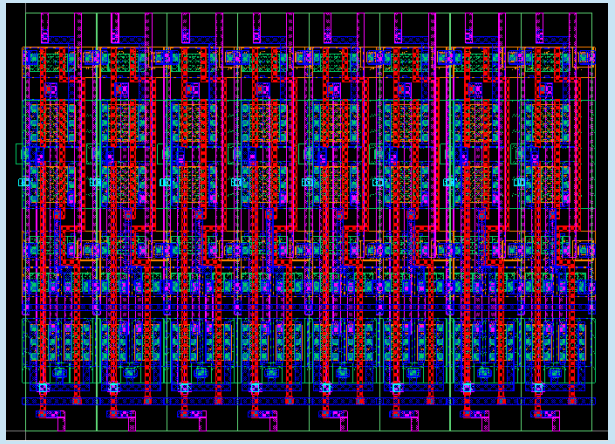
RISC-V Processor Generation

- Utilized VexRISCV to generate some RISC-V processor from existing configurations
- Uses a plugin system, so parts can be added, removed, and modified easily
- Implemented via SpinalHDL
  - HDL implemented in scala that can be converted to Verilog or VHDL
- Will enable our team to insatiate custom RISC-V cores in the user space

Top Image (Avatar of the owner of SpinalHDL): https://avatars.githubusercontent.com/u/10659437?s=200&v=4
Bottom Image (RISC-V Logo): https://upload.wikimedia.org/wikipedia/commons/thumb/9/9a/RISC-V-logo.svg/330px-RISC-V-logo.svg.png

OpenRAM Generation

- Static RAM (SRAM) necessary for processor to do useful work
- Can lay out by hand, but…
  - Time consuming
  - Error prone
  - Likely not as area efficient
- OpenRAM allows configurable SRAM generation
- Has some known issues, currently working through them
  - Alternative is using D flip-flops for RAM

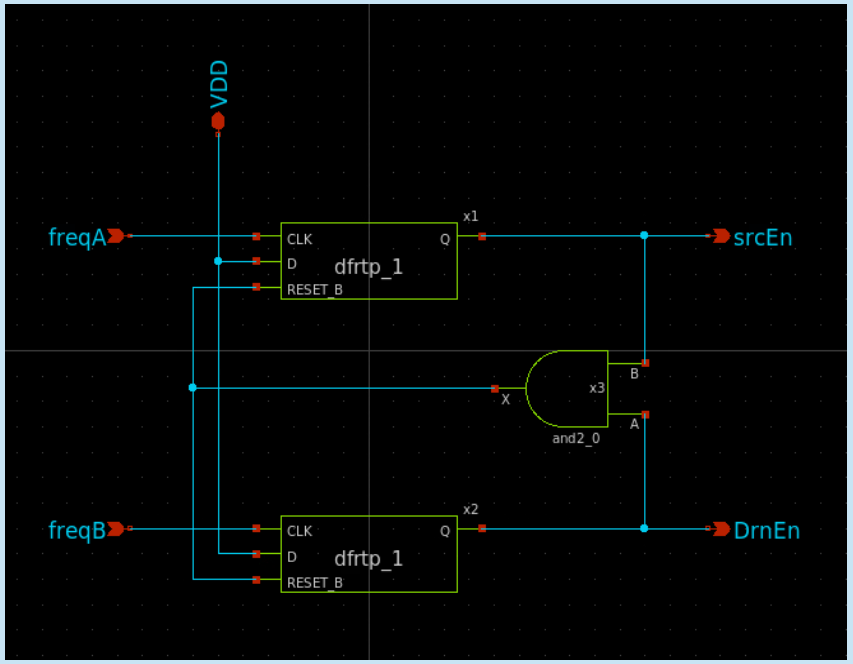


RAM Layout: https://ai2-s2-public.s3.amazonaws.com/figures/2017-08-08/2931f5cf2e33121fa75d759d8d83293dbf28bcc2/26-Figure3.2-1.png

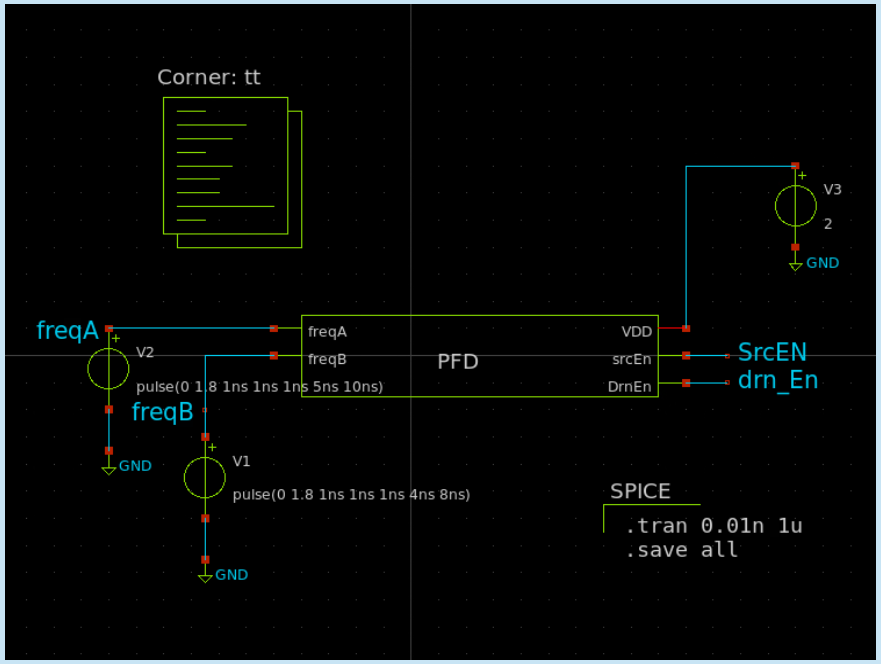
Phase Locked Loop PFD Prototype

- Phase Frequency Detector (PFD):
  - Detects if the two input signals have a phase difference

Schematic



Testbench



Conclusions

- Many key components have already had some development work completed
- So far, what we are attempting to do seems possible within technology constraints
- Will continue to evaluate, may have to make changes especially as more things are combined together
  - Certain things may work in isolation but take up too much space to co-exist