/CprE/SE 491 WEEKLY REPORT 10

11/14/2024 – 11/21/2024

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

  This week, the security sub team finished the security analysis for the microcontroller. The digital sub team continued debugging the RISC-V generation. The analog sub team met with Professor Neihart and discussed the PLL testing plan as well as possible considerations when designing each component.

  - **Past week accomplishments**
    - **Noah**
      - Determined which divider the PLL will use. Characterized parts of the PLL. Developed PLL testing plan.
    - **Nolan**
      - I Continued to learn the scala programming language so I can create plugins for the VexRISCV processor.
        - The processor uses SpinalHDL, which is implemented in scala.
    - **Nathan**
      - Wrote sample test plan for digital hardware
      - Looked into utilization for hardened 2x2 crossbar
    - **Will**
      - Mostly finished security analysis for the microcontroller

- **Ibram**
  - Decided on which divider circuit topology is better for the PLL that we are implementing. Researched and discussed PLL testing plan with Professor Neihart.
- **Ethan**
  - Researched RF module security, specifically on tampering resistance and authentication methods at the hardware level. Continued security analysis of side channel attacks on microcontrollers and countermeasures.
- **All Team Members:**

- **Pending issues**
  - **Nolan**
    - The VexRISCV tests do not pass currently. This is not required to work, but would be nice to see working so we can verify that the generated processor actually works before putting it into the user area.
  - **Nathan**
  - **Ibram**
  - **Will**

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Noah	PLL testing, characterization. Divider decision	11	60
Will	Mostly finished security analysis	6	44
Ethan	RF module security (tampering & authentication) and microcontroller security (side channel attacks)	8	44
Ibram	PLL testing and characterization. Divider circuit topology decision	10	47
Nathan	Digital hardware testplan, investigated crossbar utilization, created final presentation headers	6	53.5
Nolan	Scala learning for VexRISCV plugin development	6	55

- **Plans for the upcoming week**
  - **Will**

        - Organize security analysis to be more presentable and add it to the design document.
    - **Nathan**
        - Finish test plan for digital side
        - Expand design document with new content
    - **Ibram**
        - Work on the design document and presentation
        - Make a thorough PLL testing plan
    - **Nolan**
        - Wrap up the scala learning (I am getting fairly close)
        - Implement a wishbone interface using the VexRISCV plugin system.
        - Import the processor in the user area and run hardening.
    - **Ethan**
        - Finalize security appendix with RF security research
        - Finish organizing senior design website
    - **Noah**
        - Update design doc with PLL stuff, create presentation

- **<u>Summary of weekly advisor meeting</u>**

This week, we mainly discussed the divider circuit topology and which one would be nominal for our PLL design requirements. We also discussed the testing plan for the digital and analog components of our design. Professor Duwe gave us advice on how to successfully present our design in front of the faculty members.