EE/CprE/SE 491 WEEKLY REPORT 2

9/20/2024 – 9/27/2024

Group Number: 27

Project title: Open-Sourced Radio Microcontroller

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

This week, our team focused on researching existing radio microcontrollers. Some team members researched different security protocols to encrypt transferred data. Most team members researched high level diagram of the analog and the RF hardware that would enable data transfer via Bluetooth. We met with Professor Neihart with the presence of Professor Duwe and half of our group members to discuss project scope and expectations from the analog/ RF perspective. Some team members looked into the Caravel tutorials provided by ISU Chip Fab to get a basic understanding of how to write code for the RISC V processing and put custom hardware descriptions in the user area.

- **Past week accomplishments**
  - **Noah**
    - Watched efabless video tutorials
    - Researched the Ti CC2674R10 multiprotocol Micro Controller to determine the general data path through an RF module
      - Researched how the Ti's Digital PLL could be used
    - Researched a novel 2.4GHz RF transmitter to determine how data travels from the CPU to the antenna
    - Compiled finding into block diagram of parts worth considering

- **Nolan**
    - Got the blink Caravel example to run and played around with the code a bit.
    - Looked into the contents of the Verilog file for blinky to understand how hardware in the user area talks with the rest of the Caravel board.
    - Started going through the UART tutorial for the Caravel board.
    - Read through some of the referenced Caravel documentation and the documentation of components on the Caravel board.
    - Read through my CPR E 281 book's Verilog reference and checked out a Verilog book that the CPR E 281 book referenced to delve deeper into Verilog.
- **Nathan**
    - Got simple blink example working on efabless board
    - Set up and attended meeting with Dr. Neihart about RF side of radio
    - Researched details of efabless CPU and peripherals
    - Researched details of Bluetooth Licensing and modulation
- **Will**
    - Researched some security measures implemented in the Bluetooth protocol.
    - Attended the meeting with Dr. Neihart.
- **Ibram**
    - Researched different analog and RF components of Bluetooth
    - Looked at different online resources and books to understand more about RF design
    - Attended the inperson meeting with Prof. Duwe and Prof. Neihart.
- **Ethan**
    - Researched BLE security modes and protocols.
    - Researched Authenticated pairing with Bluetooth utilizing ECDH and AES-CCM encryption.
    - Started caravel tutorials and started working on on-boarding for the efabless board.
- **All Team Members:**
    - Compiled findings into presentation for Dr. Duwe
    - Some of us met with Dr.Neihart to learn more about the analog components of the radio transmitter and wireless protocols.

- **Pending issues**
    - Scheduling more meetings outside of class and advisor meetings to continue to catch up and share findings. Hard to work around everyone's busy schedules,

projects, clubs, jobs, etc.

o **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Noah	Efabless tutorial, Ti Multiprotocol Research, Novel 2.4GHz transmitter research, data flow understanding	5	7
Will	Researched some security measures implemented within the Bluetooth protocol.	2	4
Ethan	Researched BLE security protocols, modes, and processes. Started efabless tutorials. Researched encryption standards used in BLE.	2	4
Ibram	Researched different RF resources for Bluetooth	2	4
Nathan	Researched CPU and peripherals and Bluetooth licensing, learned about RF of Bluetooth and Zigbee with Dr. Neihart.	3	6
Nolan	Went through some of the Caravel tutorials and got code to run on the RISC V processor and a hardware description to be implemented in the user area. Read through some of the Caravel documentation briefly. Refreshed myself with Verilog and found a good reference book from the library to expand my Verilog knowledge.	3.5	4.5

o **Plans for the upcoming week**
- **Will**
  - Research more about the security of Bluetooth and Zigbee
- **Nathan**
  - More research into CPU and peripherals
  - Continue working examples up through adder example
- **Ibram**
  - Get started with efabless tutorials and tools
  - Research RF/analog documentation of earlier and existing Bluetooth protocols
- **Nolan**

- Do some research on Zigbee and learn about what we have already researched.
- Look into how to interface and use the Caravel platform, beyond what the tutorials demonstrate.
    - Learn about the wishbone bus on the Caravel platform.
    - Learn how Verilog code we write interacts with the programs we write for the RISC V processor.
    - Learn about how to interface with the GPIO subsystem and all other subsystems on the Caravel board beyond what the tutorials state.
- Go through the Verilog book I got to learn more about Verilog and practice implementing more complicated logic components in Verilog.
- **Ethan**
    - Research security protocols and practices specifically utilized by Zigbee.
    - Do more research on Zigbee and BLE in general.
    - Continue working on efabless tutorials and on-boarding.

o **Summary of weekly advisor meeting**
- We discussed the pros and cons of Bluetooth and Zigbee as well as the possibility for a multiprotocol RF module. Duwe wanted to know what costs are associated with each standard. We discussed the capabilities of the RISC-V processor, as well as additional compute features should we design an additional core for the RF module. We began investigating the security components of each protocol as well, focusing on Bluetooth this week. Lastly, we covered the general layout and requirements of an RF module.