EE/CprE/SE 491 WEEKLY REPORT 3

9/27/2024 – 9/3/2024

Group Number: 27

Project title: Open-Sourced Radio Microcontroller

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

  This week we focused on researching four things; ZIgbee certification, Zigbee security, the on-board wishbone bus, and PLL design. The are several unclear questions about CSA's Zigbee certification process so one of our goals next week is to contact them to learn more. We learned more about the requirements of the Zigbee standard and its sub-GHz frequency options. Lastly, we discussed the design of PLLs for use in the RF module. We are looking at what design constraints exist to build a silicon PLL.

  - **Past week accomplishments**
    - **Noah**
      - Worked on Adder tutorial for the Efabless process. Read through the "Radio Design for Amateurs" textbook. Discussed how the PLL worked. Researched how PLL's operate and what each component does.
    - **Nolan**
      - Researched the Zigbee licensing/certification details
      - Read through more of the Caravel documentation to understand the user project structure and overall architecture of the Caravel platform
      - Read through first part of my Verilog book and created a full adder with a testbench that utilizes some new Verilog concepts I learned

- **Nathan**
  - Continued work on tutorial examples (UART and Adder) to understand tool flow
  - Researched Wishbone bus specification
  - Started sketching block diagram for memory mapped devices
- **Will**
  - Researched the security features in ZigBee protocols at each network layer
- **Ibram**
  - Researched the different components that a Phase locked loop (PLL) has which includes a voltage-controlled oscillator, digital divider, charge pump, and a phase frequency detector.
- **Ethan**
  - Continued working on onboarding process for Chip ISU. Researched wireless protocols and security for ZigBee Standard, ZigBee 3.0 Standard, and IEEE 802.15.4 wireless standards/network model.
- **All Team Members:**
  - Contributed to the weekly advisor meeting slides, which are attached to the Canvas submission for this assignment.

- **Pending issues**
  - UART not connecting on Linux machine to test boards, blocking tutorial completion

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Noah	Adder Example, PLL research, Reading radio design book.	4	11
Will	ZigBee security research, review encryption methods.	3.5	7.5
Ethan	Wireless security research, onboarding process for Chip ISU, caravel onboarding.	3	7
Ibram	PLL component implementation	3	7
Nathan	Continued tutorial work, read up on Wishbone memory bus, started looking into block diagram	3.5	9.5
Nolan	Researched Zigbee licensing/certification, learned more Verilog, learned more about the Caravel platform.	3.2	7.7

- **Plans for the upcoming week**
  - **Will**
    - Do Chip ISU tutorials, learn more about where encryption would be implemented in block diagram, ask Dr. Gulmezoglu about wireless hardware security.
  - **Nathan**
    - Block diagram work for preliminary design
    - Look into issues with tutorials and get them resolved
  - **Ibram**
    - Understand calculations behind each component.
    - Design limits of each PLL component.
    - Look through the documentation for the ISU Chip Forge.
  - **Nolan**
    - Contact Zigbee about certification process and involved costs.
    - Continue to learn more Verilog so I am comfortable with more complicated Verilog code, which will be present as we start to put hardware descriptions in the user space.
    - Start developing a block diagram with Nathan that describes the overall design we will be putting in the user space.
    - Digging into the Caravel platform more.
  - **Ethan**
    - Finish tutorials and onboarding from Chip ISU, continue messing around with caravel. Discuss hardware security options with Dr. Gulmezoglu
  - **Noah**
    - Constraints of PLL design, how PLL's can fail.

- **Summary of weekly advisor meeting**

Discussed findings around Zigbee licensing and security, Wishbone memory bus, PLL design. Dr. Duwe suggested generating a complete block diagram for the user space, researching PLL design to figure out more details regarding pitfalls, and contacting Zigbee about licensing costs and requirements.