EE/CprE/SE 491 WEEKLY REPORT 4

10/3/2024 – 10/10/2024

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

  This week's primary goal was to create a preliminary block diagram of the complete system, then trim the diagram to create a minimal implementation that we could attempt to create throughout the course. We learned more about the different components that need to be included in the system and some details about the inner functions of these components. Additionally, we are closing in on deciding on what waveform we will implement, which will have large impacts on the rest of the design, especially from an analog perspective.

  - **Past week accomplishments**
    - **Noah**
      - Created diagrams for RF design, minimum implementation, and stretch goals.
      - Analyzed the difference between analog and digital PLLs with Ibram and determined that we will implement an analog PLL.
      - Determined that the primary deliverable for the RF module from our team will be an analog PLL capable of locking to the sub-GHz frequencies of the Zigbee wireless protocol.
    - **Nolan**

        - Created a high-level block diagram for the RISC-V cores we are planning to utilize in the user space. These are very high-level and lower-level diagrams will be created in the future to cover more of the Caravel-specific details.
        - Read through the RISC-V RV32I instruction set to understand what instructions we would be implementing and to get some insight on what logic elements we would need to create a RISC-V core.
        - Did a deep dive into how to interface with the Caravel GPIO. Documentation was sparse and sometimes conflicting, but I was able to get a decent understanding via the ChipForge tutorials. In the future, I will be looking at the Caravel project source to get a better understanding of how all the GPIO works since the definitions must be in there.
        - Worked through the ChipForge adder tutorial.
    - **Nathan**
        - Created high level block diagram for digital components of system
        - Worked on scoping design to try and find a minimum viable product that can be created in the time allotted for the course
        - Investigated details of RISC-V architecture and DMA principles
    - **Will**
        - Progressed on the ISU ChipForge tutorials on git.
        - Looked into hardware implementations of AES encryption.
        - Reached out to Dr. Gulmezoglu to see if he had any knowledge on wireless encryption methods.
    - **Ibram**
        - Researched different phase locked loop (PLL) implementation
        - Researched high level diagrams of the radio frequency component of Bluetooth
    - **Ethan**
    - **All Team Members:**

- **<u>Pending issues</u>**
    - Nolan
        - Some of the Caravel documentation seems to not be consistent with itself and is overall confusing. There exists documentation about the Management SOC that describes things like GPIO that seems to conflict with other GPIO documentation I found in the overall Caravel documentation (the Management SOC documentation has its own page which is found here: https://caravel-mgmt-soc-litex.readthedocs.io/en/latest/). I need to reach out and get some

assistance on how to make sense of this documentation.

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Noah	Revised Block Diagram of RF module, Scoped RF part of project, and Investigated Analog vs. Digital PLLs	5	16
Will	Started ChipForge git tutorials, further researched hardware implementation of encryption methods	3	10
Ethan			
Ibram	Overview hardware implementation of Bluetooth Researched different PLL structures	8	15
Nathan	Digital block diagram creation, RISC-V and DMA invesitgation	6	15.5
Nolan	Created a high-level block diagram of a RISC-V core. Read through some of the RISC-V RV32I instruction set. Read through more of the ChipForge Caravel tutorials and read through some of the Caravel documentation, specifically on GPIO and UART.	4	11.7

- **Plans for the upcoming week**
  - **Will**
    - Finish the ChipForge the ChipForge tutorial on git and experiment more to gain a deeper understanding.
    - Research hardware implementations of AES encryption enough to be confident in my ability to implement it in our own design.
  - **Nathan**
    - Redo block diagrams considering comments from Dr. Duwe in advisor meeting
    - Investigate OpenRAM tool to shape memory requirements
  - **Ibram**
    - Research ZigBee hardware requirements as its RF frequency is less than 1GHz and would be easier to implement than the 2.4GHz Bluetooth drive frequency.
  - **Nolan**
    - Continue to learn about the Caravel architecture and begin to write my own custom Verilog blocks to go on the FPGA that is hooked up to a Caravel board. This will verify that I understand the architecture well.

        - Contribute to the overall block diagram of our system.
        - Contact the Connectivity Standards Alliance (CSA) to see if there is a cost associated with getting a Zigbee product certified if it is for academia purposes.
    - **Ethan**
    - **Noah**
        - Research limitations of the Efabless process for analog design and begin to determine requirements for the analog PLL.
        - Continue Caravel tutorials and focus on analog design.
        - Investigate the requirements for the reference Oscillator that acts as the input for the PLL.

- **<u>Summary of weekly advisor meeting</u>**

Unfortunately, our advisor meeting was cut a little short this week, but we presented our first block diagram of our current understanding of the project and got feedback on it from Dr. Duwe. We were originally going to go with Bluetooth as the waveform of choice for the project but after talking with Duwe he heavily encouraged us to go with ZigBee. Finally, we discussed the basics of designing the RISC-V core we want to implement in our final design. It was requested that the block diagram be redone with some changes to make the design clearer and to scope the design to a more realistic level.