EE/CprE/SE 491 WEEKLY REPORT 5

10/10/2024 – 10/17/2024

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**
  This week we spent some time revising our existing preliminary block diagram of the project. This involved removing the flash controller as it is not needed in our final design, denoting which signals were analog and which were digital, and making the individual elements more readable. In addition, the open source RAM generator, OpenRAM was researched to see what size of SRAM blocks we could generate and put into our design given our sizing constraints and the constraints of the 130nm process. Finally, more research was done for the RF components of the project. Dr. Duwe made us aware of the Efabless marketplace during our meeting, so we looked there to see if there exist any components that we could use.

- **Past week accomplishments**
  - **Noah**
    - Worked through several examples for caravel and Efabless
    - Looked at marketplace IP for PLL design
  - **Nolan**
    - Helped revise the block diagram.

        - Further looked into the Caravel harness platform by studying the project architecture, reading through some definition files and examples from Caravel and ChipForge.
        - Created (but have not tested) a custom program to store and shift a bit on the shift register hooked up to a seven segment display connected to the FPGA we have in the lab. This was to verify that I understood how to get a custom hardware design working and if I could interface with the hardware design through the management SOC. I have not been able to test this yet since a seven segment display is not hooked up to the FGPA, but I have let Greg from ChipForge know and he will be hooking one up soon.
        - Looked into how the FPGA configuration works.
    - **Nathan**
        - Investigated OpenRAM compiler for SRAM blocks on Efabless
        - Investigated theoretical RAM capacity limits
        - Helped rework block diagram for system
    - **Will**
        - Looked into hardware implementation of AES, found free open-source code for AES
    - **Ibram**
        - Looked at different ways to test PLLs and started on tutorials
    - **Ethan**
        - Worked on hardware implementation of 128-bit AES encryption utilized by the Zigbee Protocol. Looked at open-sourced code available for verilog implementations of 128-bit AES encryption. I did research and studied Verilog programming.
    - **All Team Members:**
        - Everyone this week did something different as seen above.

- **<u>Pending issues</u>**
    - **Nathan**
        - Issue building OpenRAM configurations with larger word counts
    - **Noah**
        - Determine base frequency necessary from system clock or reference oscillator
        - Find the maximum vcc that can be delivered to the vco
    - **Nolan**
        - Need the seven segment display to be hooked up to the FPGA so I can test my code out.

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Noah	Caravel tutorials, PLL IP Investigation	6	22
Will	Finished researching AES, found open-source AES code, continued chipForge tutorials	6	16
Ethan	AES hardware implementation research. Verilog research and studying.	4	14
Ibram	Fstarted the tutorials and looked at PLL testing circuit topology	4	19
Nathan	RAM capacity, RAM generation, block diagram	7.5	23
Nolan	Caravel investigations and test program development, block diagram	6	17.7

- **Plans for the upcoming week**
  - **Will**
    - Finish chip forge tutorials, research where encryption fits into the whole diagram.
  - **Nathan**
    - RISC-V core generation
    - More OpenRAM work
  - **Ibram**
    - Finish tutorials and start on designing the frequency phase detector
    - Look at the open-source components that efabless has on marketplace.
  - **Nolan**
    - Get the seven-seg hardware design and SW implementation working.
    - Further dive into the Caravel platform to fully understand all of the components and get to the point where I can easily define my own hardware implementations and software interfaces to those implementations.
    - Look into RISC-V core generation tools.
  - **Ethan**
    - ChipForge & Caravel tutorials.
    - Refresh / study Verilog more.
    - Look at other hardware security options.
  - **Noah**

- Find the max vcc that can be delivered to the vco on silicon
- Determine base frequency necessary to achieve desired frequencies
- Use these findings for to determine requirements for the PLL in the design document

- **Summary of weekly advisor meeting**

  In the meeting with Dr. Duwe this week, we presented our revised block diagram and the results of the OpenRAM investigation. Dr. Duwe presented some questions about having all the digital connections being their own wishbone lines and suggested that we take advantage of a bus architecture. In addition, Dr. Duwe made known to us that Efabless has a marketplace where we can view silicon-proven designs for components that are supported by the Caravel platform. Given this knowledge, we are looking into what the Efabless marketplace has to offer regarding RF components that we need. Finally, Dr. Duwe also suggested that we investigate customizable RISC-V core generators to instantiate the RISC-V cores we desire to put in the user area.