EE/CprE/SE 491 WEEKLY REPORT 6

10/17/2024 – 10/24/2024

Group Number: ***27***

Project title: ***Open-Sourced Radio Microcontroller***

Client &/Advisor: ***Dr. Henry Duwe***

Team Members/Role:
Noah: *Team Organization*
Will: *Project Management*
Ibram: *Analog Design Lead*
Nathan: *Digital Peripheral Lead*
Nolan: *CPU/Memory Architecture Lead*
Ethan: *Software Lead*

- **Weekly Summary**

  This week was primarily individual research. Some members looked through the analog and digital tutorials, some investigated the open-source RISC-V, and some investigated cyber security analysis. We have collaboratively worked on the design requirements report section, the detailed design and visuals in-class activity, and the second lighting talk presentation.

- **Past week accomplishments**
  - **Noah**
    - Worked on Caravel Analog tutorials with ISU Chip Forge
    - Investigate the design of the digital PLL used for RISC-V core in the management area to see if the resulting clock signal could be used instead of a reference oscillator.
  - **Nolan**
    - Continued developing a seven segment controller hardware description for the FPGA.

        - Created a hardware description that can be signaled from the management SOC over the logic analyzer to reset the seven segment controller, clear the seven segment display, and fill the seven segment display with all ones.
        - Looked into how to control the user clock from the Caravel clocking subsystem.
        - Read through the core Caravel Verilog file to see how the high-level Caravel design is described in Verilog. Since the documentation is sparse, this is quite an effective way to learn.
        - Read through some of the existing Caravel test C files for the management SOC.
    - **Nathan**
        - Researched open-source RISC-V cores for project
        - More research into OpenRAM
    - **Will**
        - Started cybersecurity analysis at various points in our design.
    - **Ibram**
        - Successfully got xschem to work and was able to simulate the inverter.
        - Worked on a few digital tutorials and got them working.
    - **Ethan**
        - Started a cybersecurity analysis along with Will. Studied feasibility of different encryption protocols in hardware.
    - **All Team Members:**

- **Pending issues**
    - **Nathan**
        - Issue building OpenRAM configurations with larger word counts
    - **Noah**
        - Determine base frequency necessary from reference oscillator
        - Find the maximum vcc that can be delivered to the vco
    - **Nolan**

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Noah	Researched the DPLL implementation, analog caravel tutorials	6	28

Will	Investigated security implications, ChipForge tutorials	5	21
Ethan	Security analysis of system. Research on different encryption methods. Chip Forge & Caravel tutorials.	4	18
Ibram	Worked on analog and some digital tutorials.	4	23
Nathan	OpenRAM and RISC-V investigation	6	29
Nolan	Continued developing my seven segment hardware design and management SOC driver for it. Looked into how to configure the user clock from the Caravel clocking subsystem.	8	25.7

- **Plans for the upcoming week**
  - **Will**
    - Continuing cybersecurity analysis.
    - Look into ZigBee Key sharing
  - **Nathan**
    - Try and resolve OpenRAM issue
    - More work with experiments and tutorials to learn tooling
  - **Ibram**
    - Start designing the frequency phase detector (FPD) with xschem
  - **Nolan**
    - I can fill and clear the seven segment displays currently from the FPGA, but I still need to modify the hardware description and driver SW to enable the displaying of numbers.
    - Need to look into the clocking subsystem more to determine how we can configure it.
    - Continue to read into the Caravel Verilog design to fully understand what we have access to in the user space and how the whole system works.
  - **Ethan**
    - Continue the security analysis on the system
    - Create AES block diagram
    - Continue with Caravel & Chip Forge research
  - **Noah**
    - Further experiment with analog design in Caravel
    - Define more constraints for the PLL design

- **Summary of weekly advisor meeting**

In this week's advisor meeting we went over some of our options for RISC-V generation. There were two big ones we focused on this week, the VexRISCV and the

PicoRV32. We were leaning towards the VexRISCV but Dr. Duwe wants us to do some more research before making a final decision. We were cut a little short this week but before Duwe had to leave, we looked through and discussed a software implemented PLL and tried to analyze some of the Verilog code to see what we could learn from it.